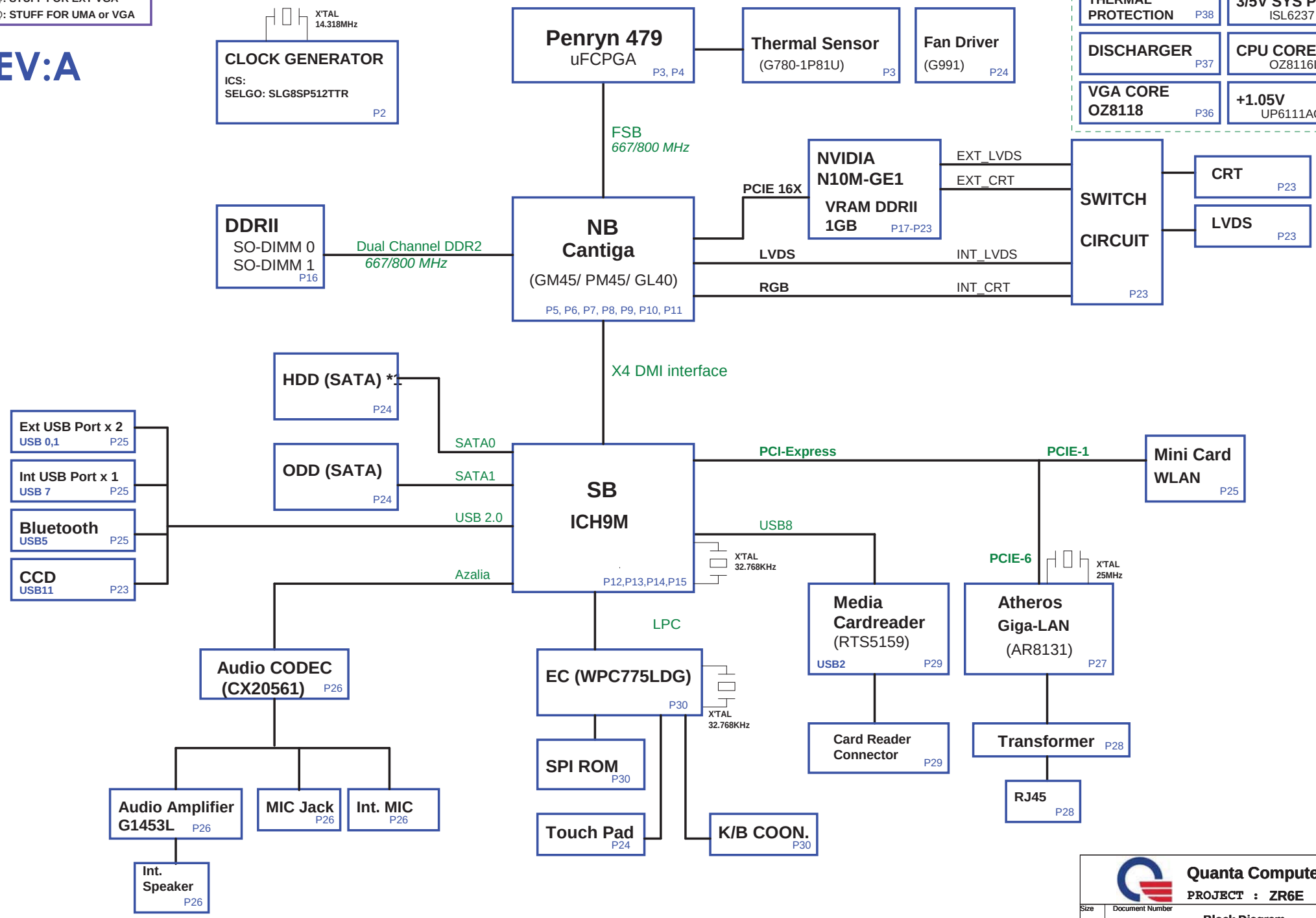
ZR6E SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

REV:A



Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	Block Diagram	1A

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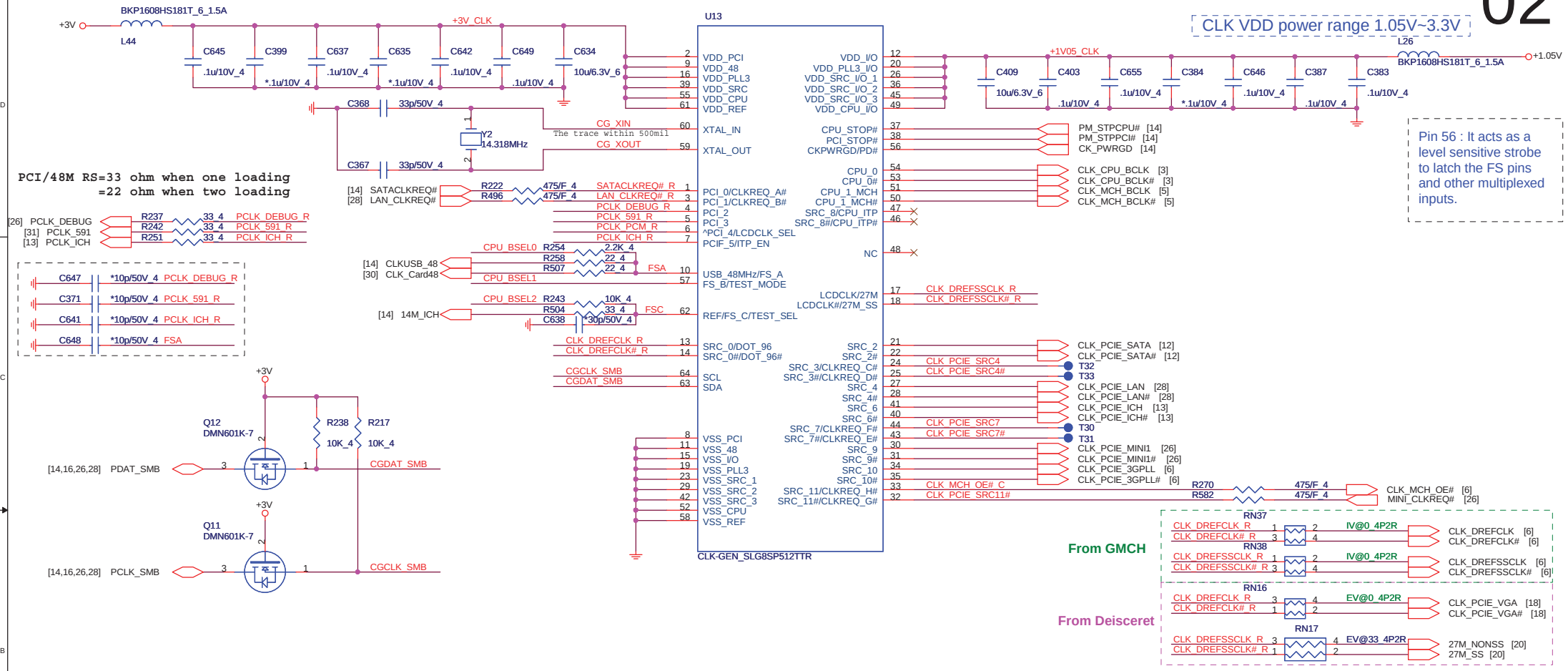
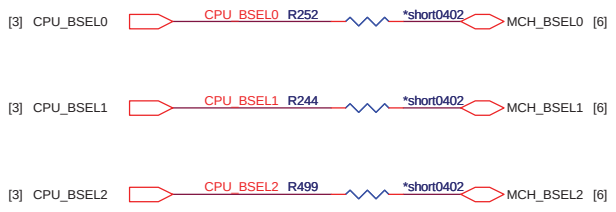
Clock Generator (CLK)

02



CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection



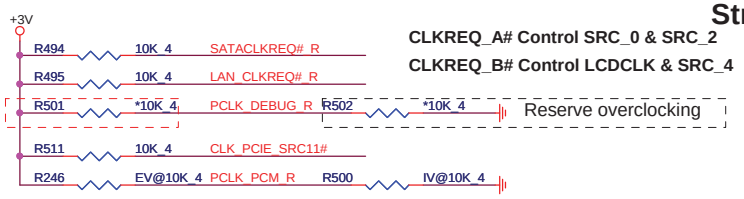
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table

CLKREQ_A# Control SRC_0 & SRC_2

CLKREQ_B# Control LCDCLK & SRC_4



Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS &SRC_0 for external graphic controller support

PCLK_ICH_R R503 10K_4

Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

CLOCK GENERATOR

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	CLOCK GENERATOR	1A

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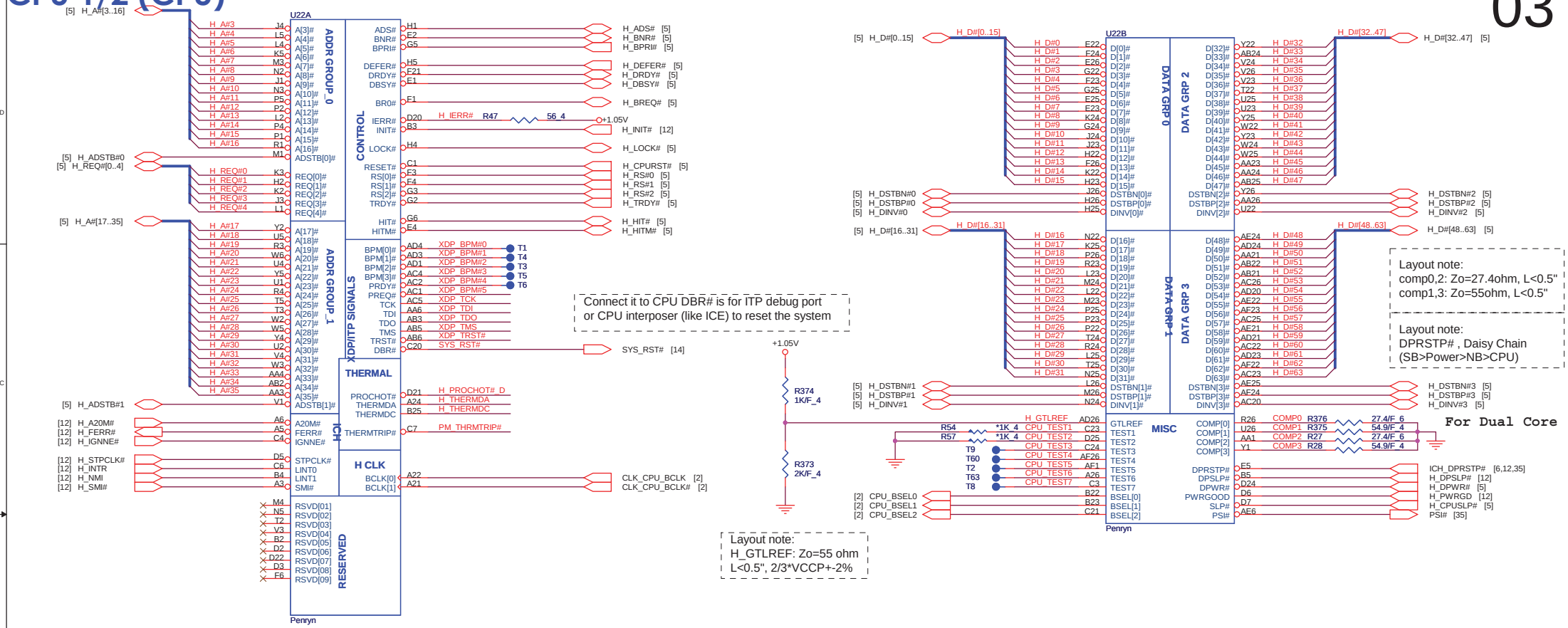
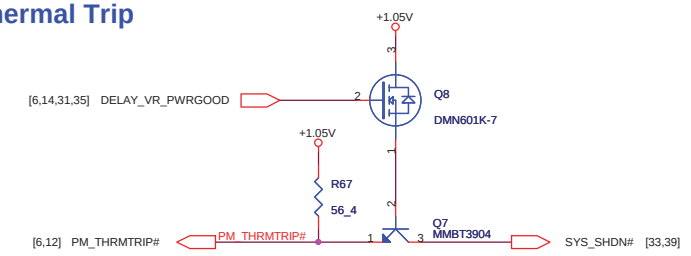
CPU 1/2 (CPU)

03



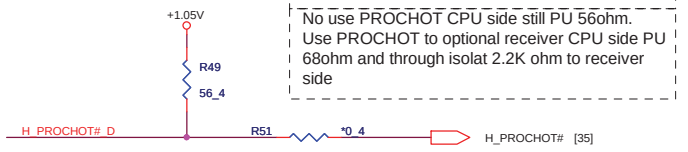
Thermal Trip



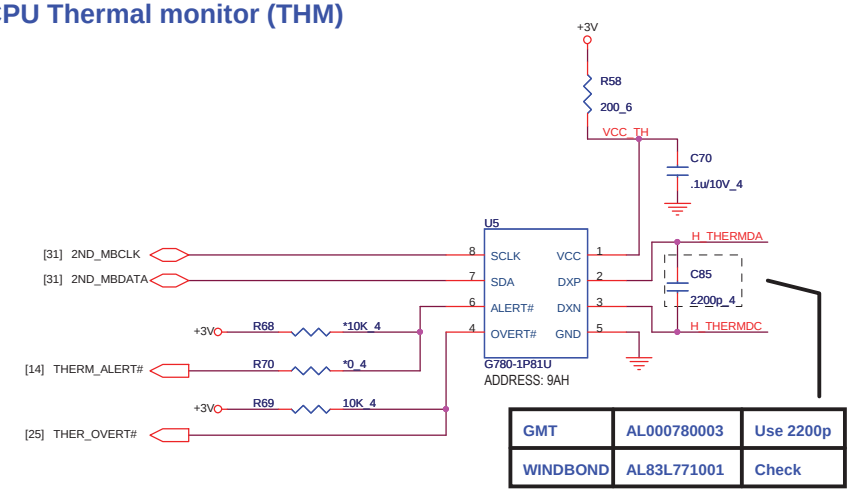
Processor hot

No use Thermal trip CPU side still PU 56ohm. Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm. Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

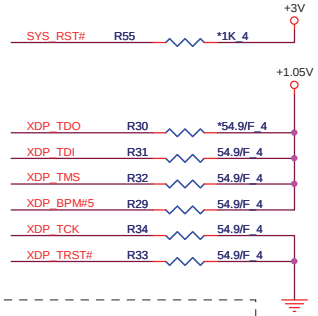


CPU Thermal monitor (THM)



GMT	AL000780003	Use 2200p
WINDBOND	AL83L771001	Check

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

Quanta Computer Inc.

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Size	Document Number	Rev
	CPU Host Bus	1A

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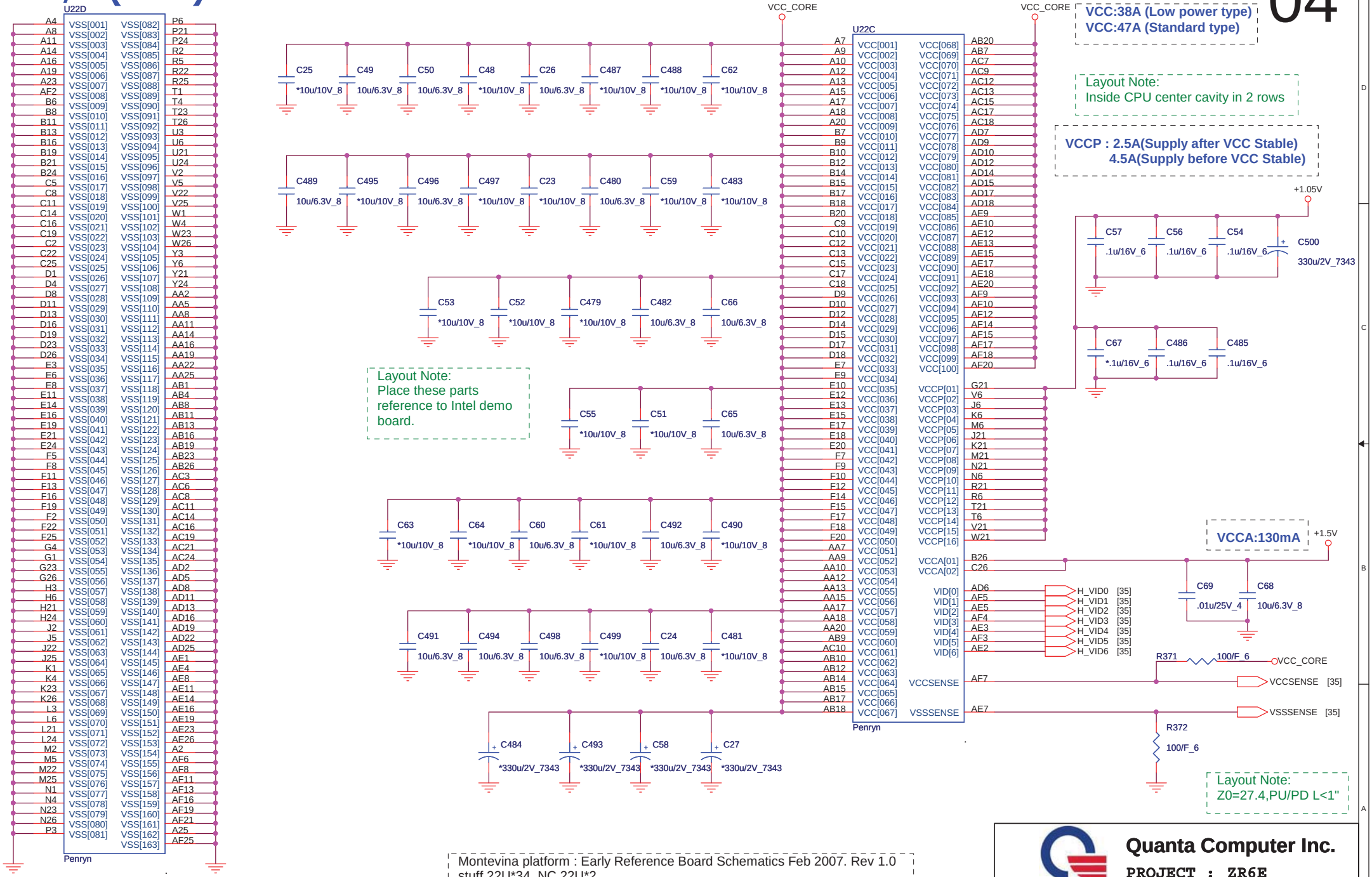
CPU 2/2 (CPU)

04


U22D
Penryn
U22C
Penryn
VCC_CORE
VCC:38A (Low power type)
VCC:47A (Standard type)
Layout Note:
Inside CPU center cavity in 2 rows
VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)
+1.05V
C57 .1u/16V_6
C56 .1u/16V_6
C54 .1u/16V_6
C500 330u/2V_7343
C67 *.1u/16V_6
C486 .1u/16V_6
C485 .1u/16V_6
Layout Note:
Place these parts
reference to Intel demo
board.
VCCA:130mA
+1.5V
C69 .01u/25V_4
C68 10u/6.3V_8
H_VID0 [35]
H_VID1 [35]
H_VID2 [35]
H_VID3 [35]
H_VID4 [35]
H_VID5 [35]
H_VID6 [35]
R371 100/F_6
VCC_CORE
VCCSENSE [35]
VSSSENSE [35]
R372 100/F_6
Layout Note:
Z0=27.4,PU/PD L<1"
Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2
Quanta Computer Inc.
PROJECT : ZR6E
Size
Document Number
CPU Power
Rev 1A
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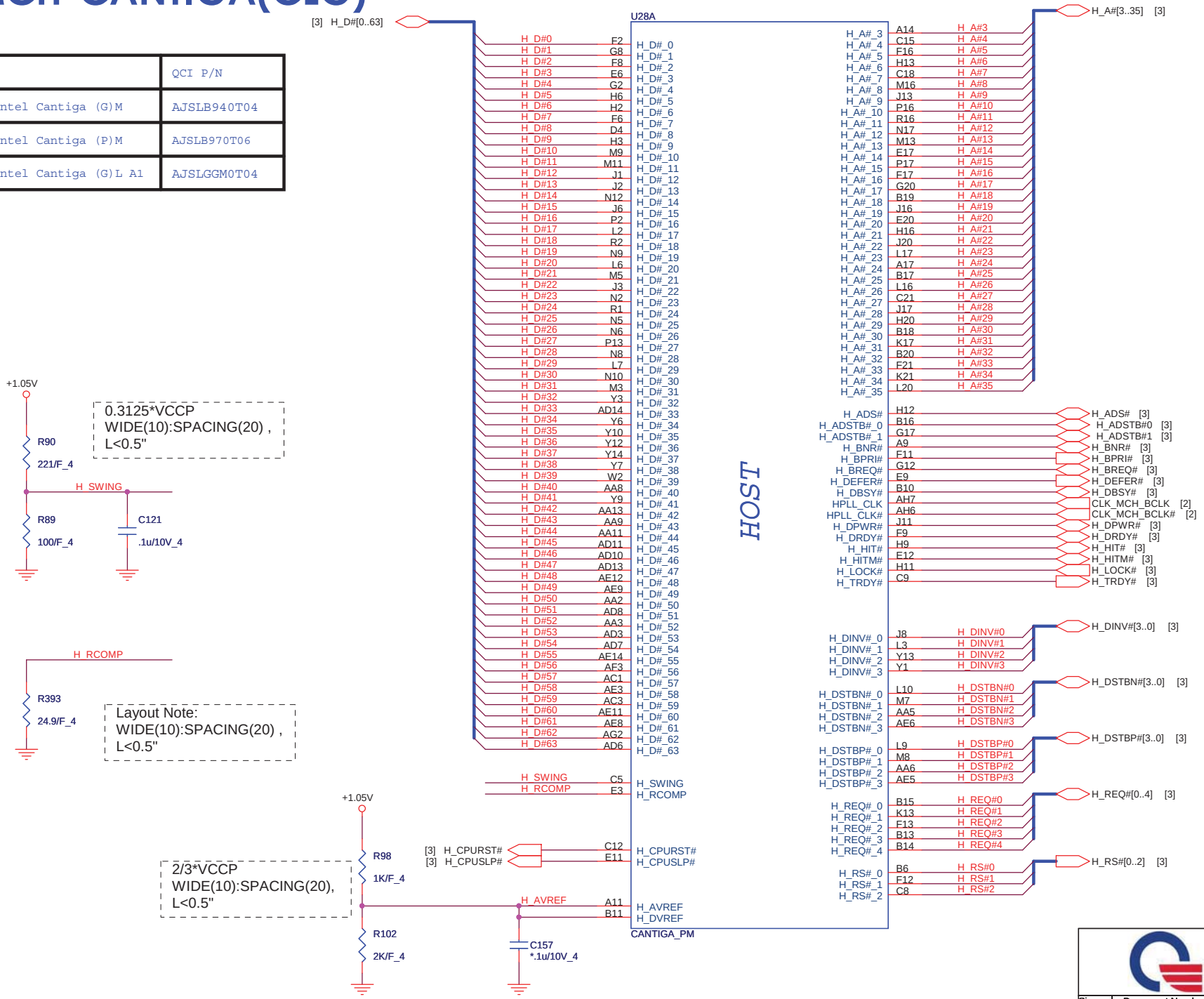
GMCH-CANTIGA(CLG)

05

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



Size	Document Number	Rev
	GMCH HOST	1A

Quanta Computer Inc.

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GMCH-CANTIGA(CLG)

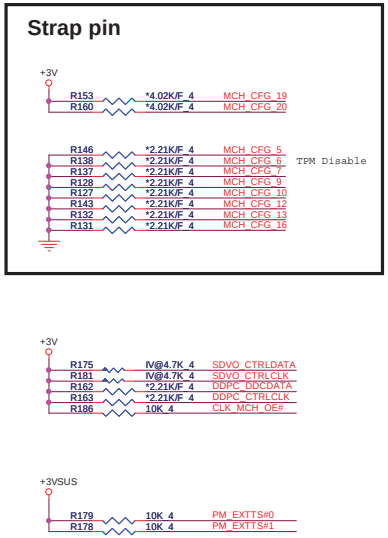
IV@
EV@

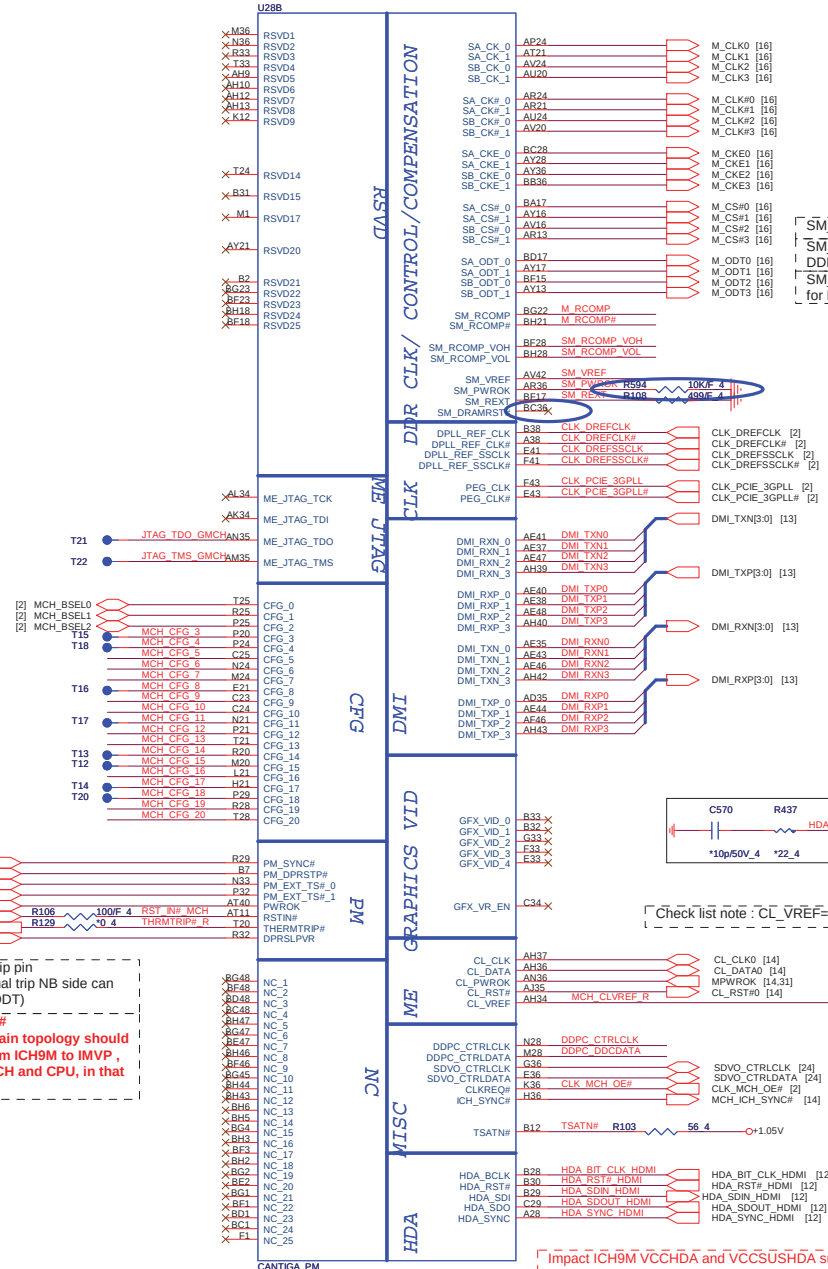
06

Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

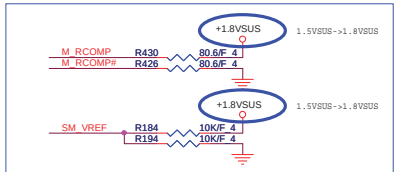
Strap pin





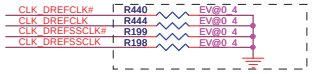
SM_VREF=0.5*VCC_SM
SM_PWROK only for DDR3.(DDR2 PD only)
SM_DRAMRST# only for DDR3.(DDR2:NC)

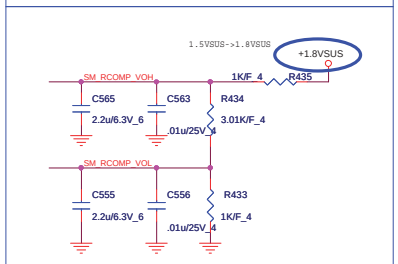
Check list note : CL_VREF=0.35V



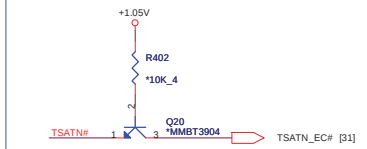
SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

INTEL FAE Suggest PD for Ext graphics





NB Thermaltrip



NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)

PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP , then to (G)MCH and CPU, in that order.

DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

If HDMI not support
HDA --> NC
VCC_HDA-->GND
Differential signal-->NC

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	GMCH DMI	1A

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GMCH-CANTIGA(CLG)

IV@
EV@
SP@

IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

U28C

[24] L_BKLT_CTRL — L32 L_BKLT_CTRL
[24] INT_LVDS_BLON — G32 L_BKLT_EN
R171 IV@10K_4 — M32 L_CTRL_CLK
+3V — R172 IV@10K_4 — M33 L_CTRL_DATA
[24] INT_LVDS_EDIDCLK — K33 L_DDC_CLK
[24] INT_LVDS_EDIDDATA — J33 L_DDC_DATA
[24] INT_LVDS_DIGON — M29 L_VDD_EN
R195 IV@2.4K/F_4 LVDS_IBG — C44 LVDS_IBG
B43 LVDS_VBG
E37 LVDS_VREFH
E38 LVDS_VREFL
[24] INT_TXLCLKOUT- — INT_TXLCLKOUT- — C41 LVDSA_CLK#
[24] INT_TXLCLKOUT+ — INT_TXLCLKOUT+ — C40 LVDSA_CLK
B37 LVDSB_CLK#
A37 LVDSB_CLK
[24] INT_TXLOUT0- — INT_TXLOUT0- — H47 LVDSA_DATA#_0
[24] INT_TXLOUT1- — INT_TXLOUT1- — E46 LVDSA_DATA#_1
[24] INT_TXLOUT2- — INT_TXLOUT2- — G40 LVDSA_DATA#_2
A40 LVDSA_DATA#_3
[24] INT_TXLOUT0+ — INT_TXLOUT0+ — H48 LVDSA_DATA_0
[24] INT_TXLOUT1+ — INT_TXLOUT1+ — D45 LVDSA_DATA_1
[24] INT_TXLOUT2+ — INT_TXLOUT2+ — F40 LVDSA_DATA_2
B40 LVDSA_DATA_3
A41 LVDSB_DATA#_0
H38 LVDSB_DATA#_1
G37 LVDSB_DATA#_2
J37 LVDSB_DATA#_3
B42 LVDSB_DATA_0
G38 LVDSB_DATA_1
F37 LVDSB_DATA_2
K37 LVDSB_DATA_3

LVDS

SP@ TV_A/B/C
For IV: 75ohm
For EV:0ohm

R147 SP@75_4 — INT_TV_COMP — F25 TVA_DAC
R136 SP@75_4 — INT_TV_Y/G — H25 TVB_DAC
R151 SP@75_4 — INT_TV_C/R — K25 TVC_DAC
H24 TV_RTN
C31 TV_DCONSEL_0
E32 TV_DCONSEL_1

[24] INT_CRT_BLU — INT_CRT_BLU — E28 CRT_BLUE
[24] INT_CRT_GRN — INT_CRT_GRN — G28 CRT_GREEN
[24] INT_CRT_RED — INT_CRT_RED — J28 CRT_RED
G29 CRT_IRTN
[24] INT_CRT_DDCCLK — H32 CRT_DDC_CLK
[24] INT_CRT_DDCDAT — J32 CRT_DDC_DATA
[24] INT_HSYNC — R158 IV@30.1_4 — HSYNC_G — J29 CRT_HSYNC
CRTIREF — E29 CRT_TVO_IREF
[24] INT_VSYNC — R165 IV@30.1_4 — VSYNC_G — L29 CRT_VSYNC

HSYNC/VSYNC serial R place close to NB

CANTIGA_PM

VGA

PCI-EXPRESS GRAPHICS

L<0.5" , If PCIE not support still connect to +VCC_PEG

+1.05V

PEG_COMPI — T37 EXP_A_COMPX — R176 49.9/F_4
PEG_COMPO — T36

PEG_RX#_0 — H44 PEG_RXN0
PEG_RX#_1 — J46 PEG_RXN1
PEG_RX#_2 — L44 PEG_RXN2
PEG_RX#_3 — L40 PEG_RXN3
PEG_RX#_4 — N41 PEG_RXN4
PEG_RX#_5 — P48 PEG_RXN5
PEG_RX#_6 — N44 PEG_RXN6
PEG_RX#_7 — T43 PEG_RXN7
PEG_RX#_8 — U43 PEG_RXN8
PEG_RX#_9 — Y43 PEG_RXN9
PEG_RX#_10 — Y48 PEG_RXN10
PEG_RX#_11 — Y36 PEG_RXN11
PEG_RX#_12 — AA43 PEG_RXN12
PEG_RX#_13 — AD37 PEG_RXN13
PEG_RX#_14 — AC47 PEG_RXN14
PEG_RX#_15 — AD39 PEG_RXN15 — PEG_RXN[15:0] [18]

PEG_RX_0 — H43 PEG_RXP0
PEG_RX_1 — J44 PEG_RXP1
PEG_RX_2 — L43 PEG_RXP2
PEG_RX_3 — L41 PEG_RXP3
PEG_RX_4 — N40 PEG_RXP4
PEG_RX_5 — P47 PEG_RXP5
PEG_RX_6 — N43 PEG_RXP6
PEG_RX_7 — T42 PEG_RXP7
PEG_RX_8 — U42 PEG_RXP8
PEG_RX_9 — Y42 PEG_RXP9
PEG_RX_10 — W47 PEG_RXP10
PEG_RX_11 — Y37 PEG_RXP11
PEG_RX_12 — AA42 PEG_RXP12
PEG_RX_13 — AD36 PEG_RXP13
PEG_RX_14 — AC48 PEG_RXP14
PEG_RX_15 — AD40 PEG_RXP15 — PEG_RXP[15:0] [18,24]

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

PEG_TX#_0	J41	C_PEG_TXN0	C583	.1u/10V_4	PEG_TXN0
PEG_TX#_1	M46	C_PEG_TXN1	C587	.1u/10V_4	PEG_TXN1
PEG_TX#_2	M47	C_PEG_TXN2	C591	.1u/10V_4	PEG_TXN2
PEG_TX#_3	M40	C_PEG_TXN3	C596	.1u/10V_4	PEG_TXN3
PEG_TX#_4	M42	C_PEG_TXN4	C618	EV@.1U/10V_4	PEG_TXN4
PEG_TX#_5	R48	C_PEG_TXN5	C588	EV@.1U/10V_4	PEG_TXN5
PEG_TX#_6	N38	C_PEG_TXN6	C600	EV@.1U/10V_4	PEG_TXN6
PEG_TX#_7	T40	C_PEG_TXN7	C598	EV@.1U/10V_4	PEG_TXN7
PEG_TX#_8	U37	C_PEG_TXN8	C604	EV@.1U/10V_4	PEG_TXN8
PEG_TX#_9	U40	C_PEG_TXN9	C603	EV@.1U/10V_4	PEG_TXN9
PEG_TX#_10	Y40	C_PEG_TXN10	C608	EV@.1U/10V_4	PEG_TXN10
PEG_TX#_11	AA46	C_PEG_TXN11	C594	EV@.1U/10V_4	PEG_TXN11
PEG_TX#_12	AA37	C_PEG_TXN12	C616	EV@.1U/10V_4	PEG_TXN12
PEG_TX#_13	AA40	C_PEG_TXN13	C619	EV@.1U/10V_4	PEG_TXN13
PEG_TX#_14	AD43	C_PEG_TXN14	C614	EV@.1U/10V_4	PEG_TXN14
PEG_TX#_15	AC46	C_PEG_TXN15	C593	EV@.1U/10V_4	PEG_TXN15

PEG_TXN[15:0] [18,24]

PEG_TX_0	J42	C_PEG_TXP0	C580	.1u/10V_4	PEG_TXP0
PEG_TX_1	L46	C_PEG_TXP1	C585	.1u/10V_4	PEG_TXP1
PEG_TX_2	M48	C_PEG_TXP2	C590	.1u/10V_4	PEG_TXP2
PEG_TX_3	M39	C_PEG_TXP3	C597	.1u/10V_4	PEG_TXP3
PEG_TX_4	M43	C_PEG_TXP4	C611	EV@.1U/10V_4	PEG_TXP4
PEG_TX_5	R47	C_PEG_TXP5	C586	EV@.1U/10V_4	PEG_TXP5
PEG_TX_6	N37	C_PEG_TXP6	C601	EV@.1U/10V_4	PEG_TXP6
PEG_TX_7	T39	C_PEG_TXP7	C599	EV@.1U/10V_4	PEG_TXP7
PEG_TX_8	U36	C_PEG_TXP8	C605	EV@.1U/10V_4	PEG_TXP8
PEG_TX_9	U39	C_PEG_TXP9	C602	EV@.1U/10V_4	PEG_TXP9
PEG_TX_10	Y39	C_PEG_TXP10	C609	EV@.1U/10V_4	PEG_TXP10
PEG_TX_11	Y46	C_PEG_TXP11	C595	EV@.1U/10V_4	PEG_TXP11
PEG_TX_12	AA36	C_PEG_TXP12	C617	EV@.1U/10V_4	PEG_TXP12
PEG_TX_13	AA39	C_PEG_TXP13	C620	EV@.1U/10V_4	PEG_TXP13
PEG_TX_14	AD42	C_PEG_TXP14	C615	EV@.1U/10V_4	PEG_TXP14
PEG_TX_15	AD46	C_PEG_TXP15	C592	EV@.1U/10V_4	PEG_TXP15

PEG_TXP[15:0] [18,24]

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 1Kohm to GND

For topology without the analog switch - if the total motherboard route length is less than 12", the recommended reference resistor value is 1 kΩ ±1%

CRTIREF
For IV: 1Kohm
For EV:0ohm

R161 SP@1K/F_4 CRTIREF

SP@

CRT_R/G/B
For IV: 150ohm
For EV:0ohm

R155 SP@150/F_4 INT_CRT_BLU
R154 SP@150/F_4 INT_CRT_GRN
R150 SP@150/F_4 INT_CRT_RED

Discrete Stuffed. (CRT)

HSYNC_G — R159 EV@0_4
VSYNC_G — R166 EV@0_4

CRTIREF pull down for IV cantiga 1.02k ohm/F

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	GMCH VGA	1A

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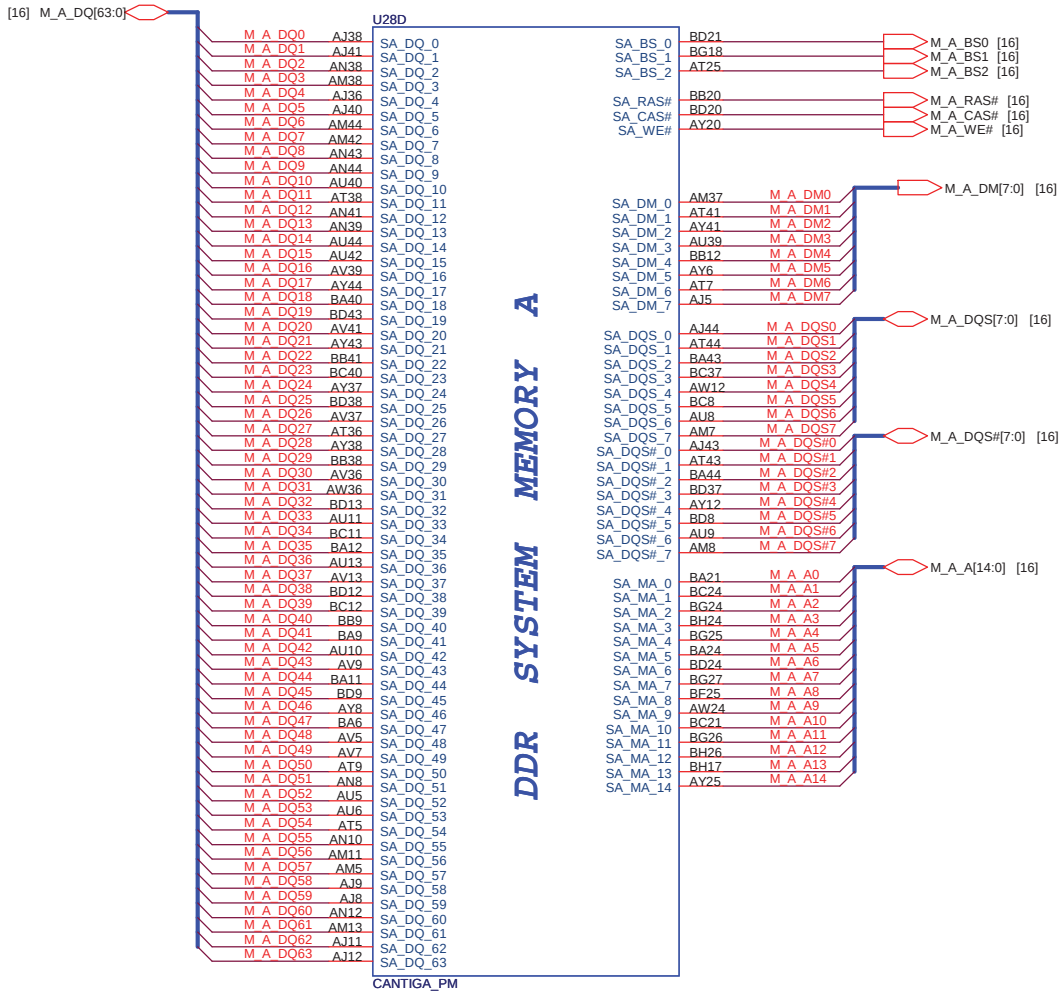
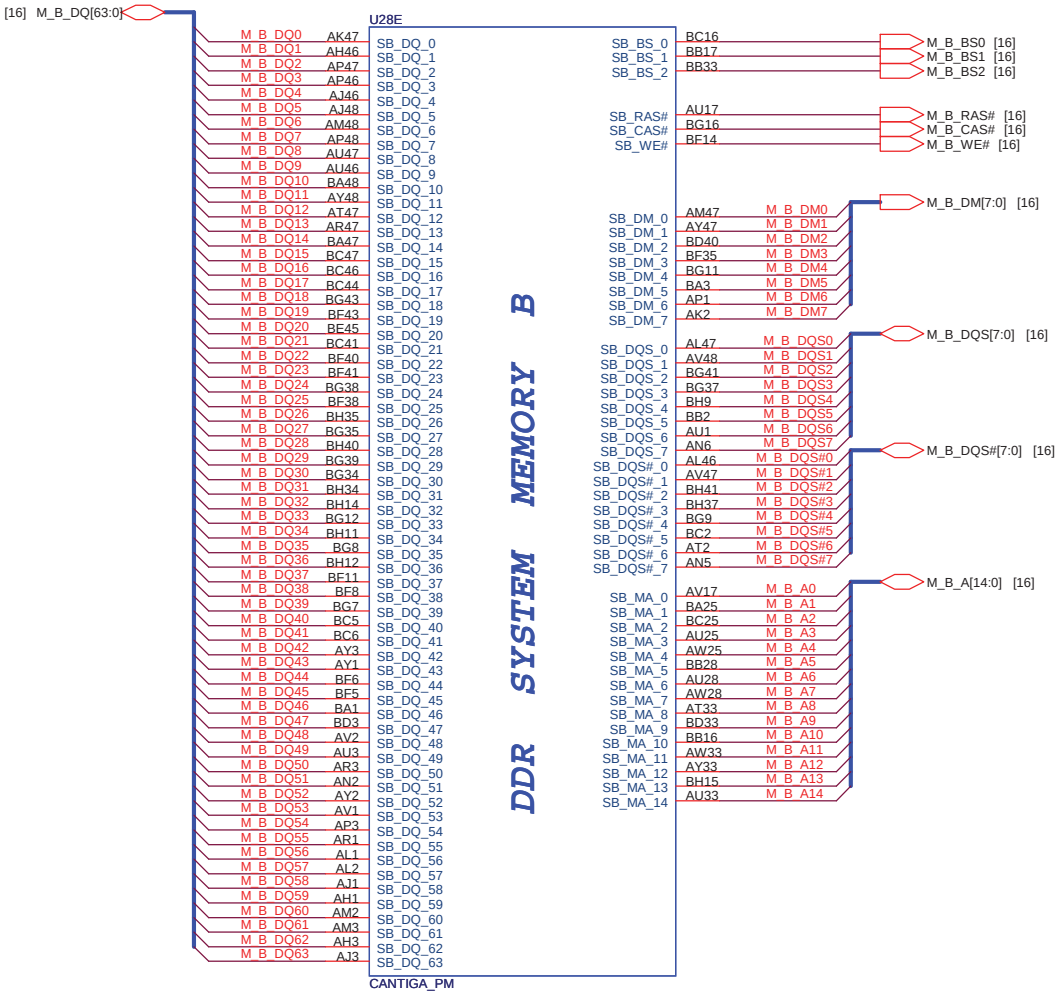
GMCH-CANTIGA(CLG)





Quanta Computer Inc.			
PROJECT : ZR6E			
Size	Document Number		Rev
	GMCH DDRII		1A
Date: Tuesday, May 19, 2009	Sheet 8 of 39		

GMCH-CANTIGA(CLG)

IV@

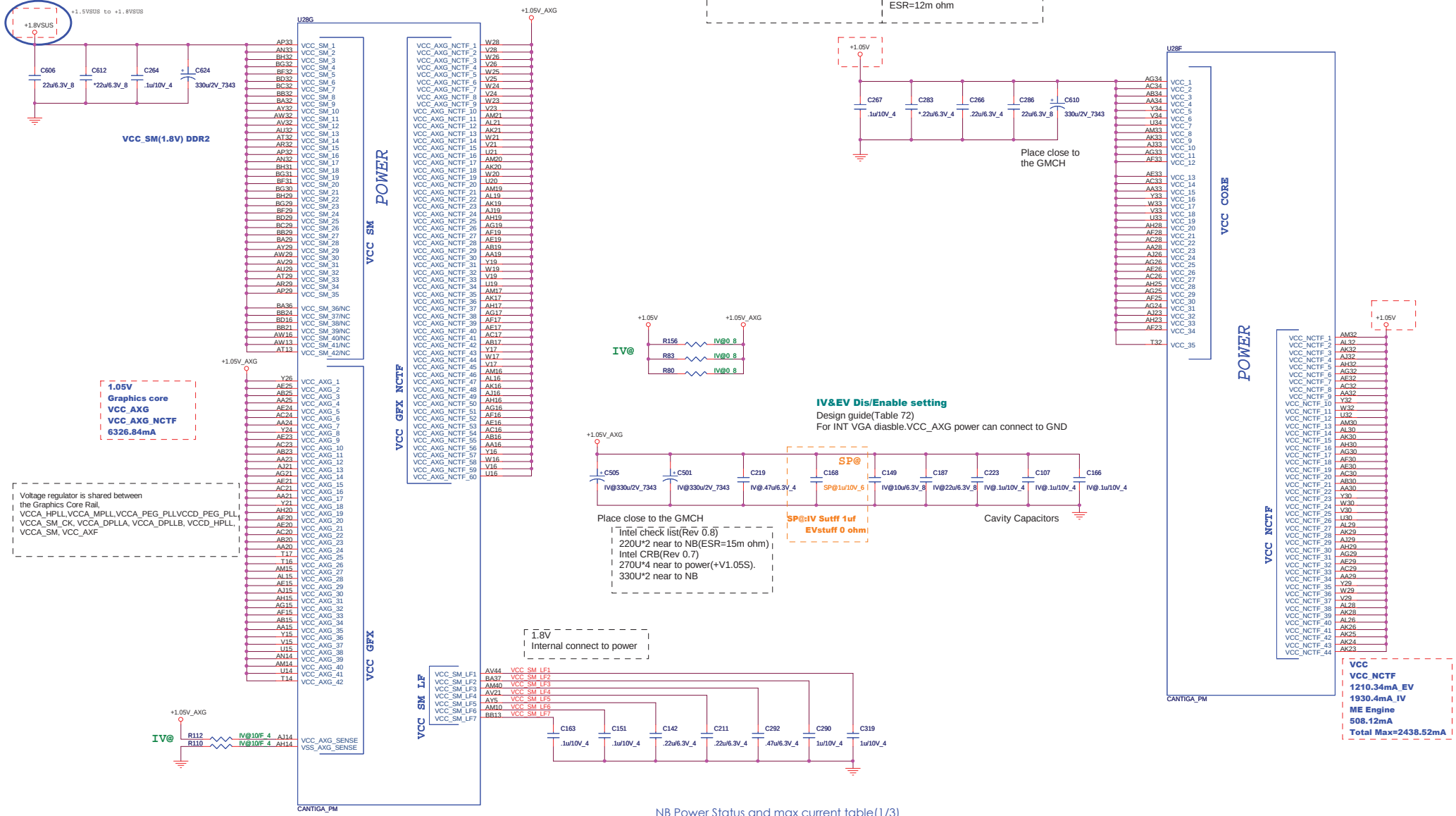
SP@

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm



1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	GMCH VCC,NCTF	1A

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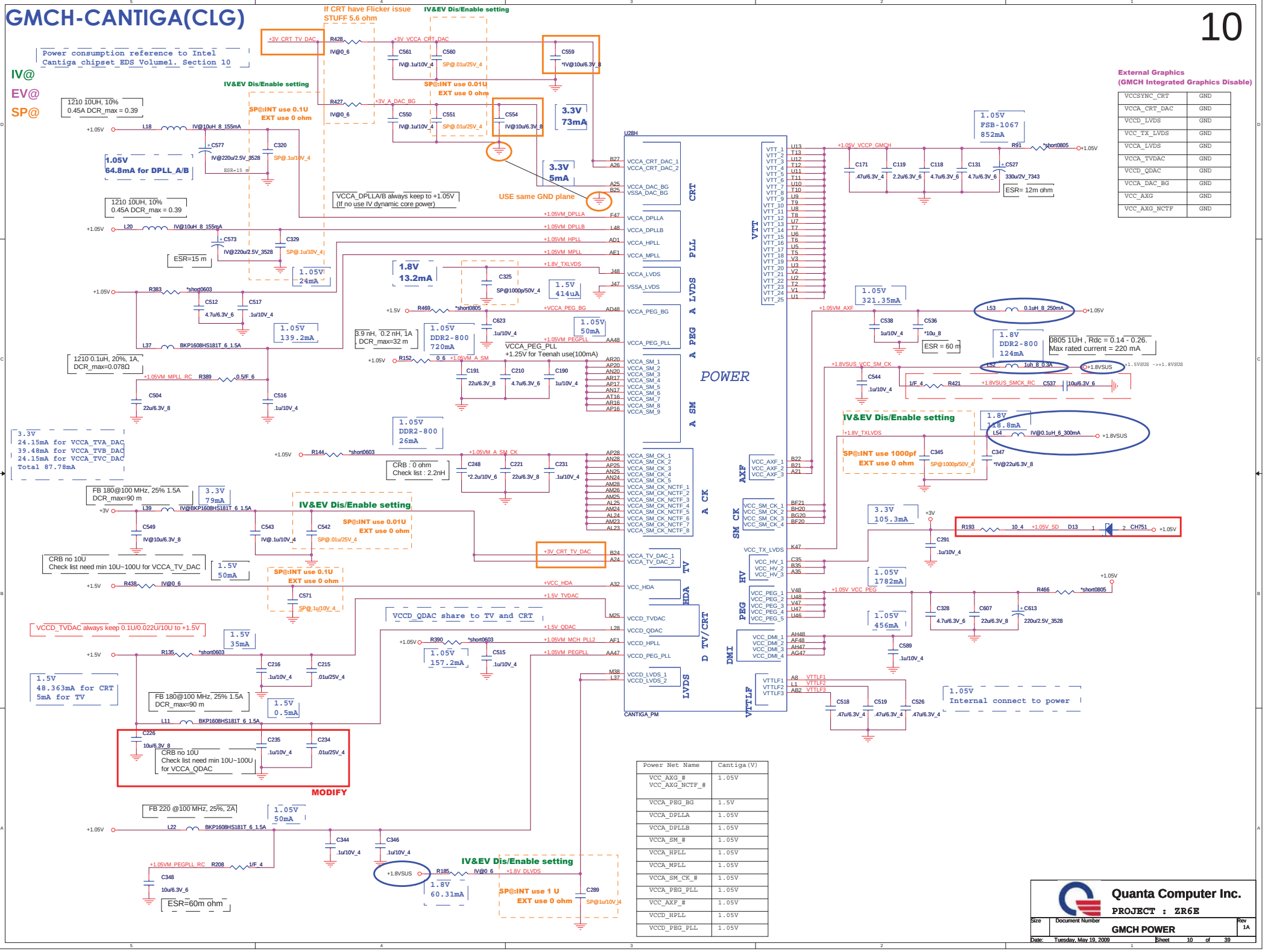
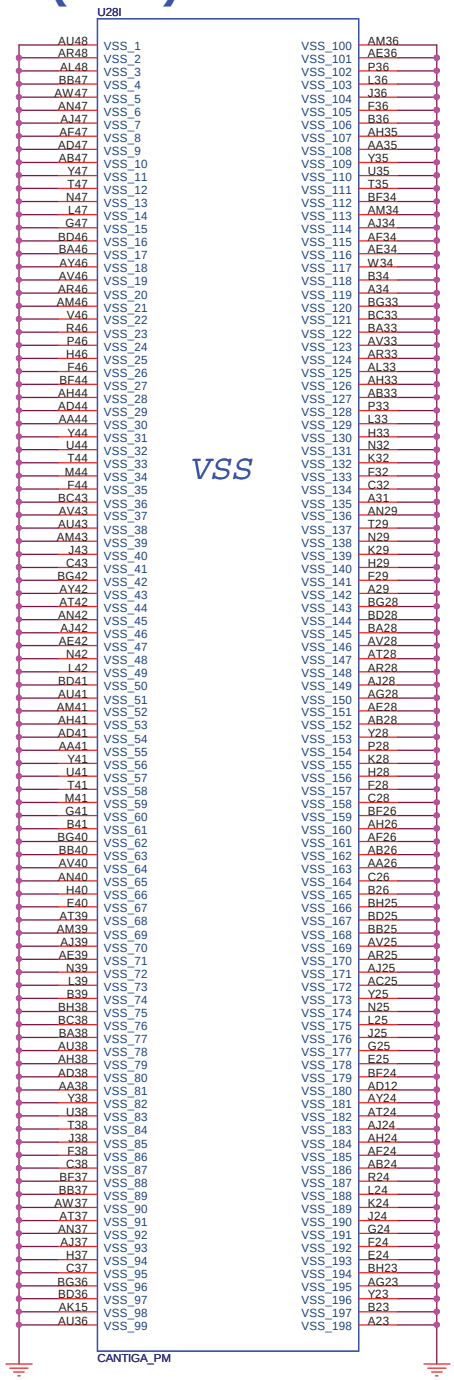
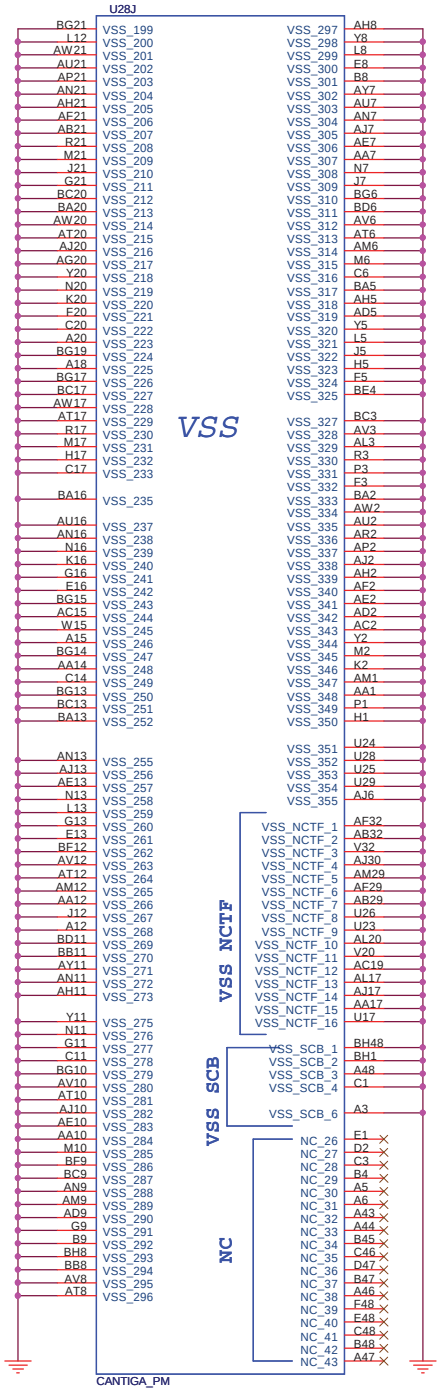
GMCH-CANTIGA(CLG)



GMCH-CANTIGA(CLG)





Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	GMCH VSS	1A

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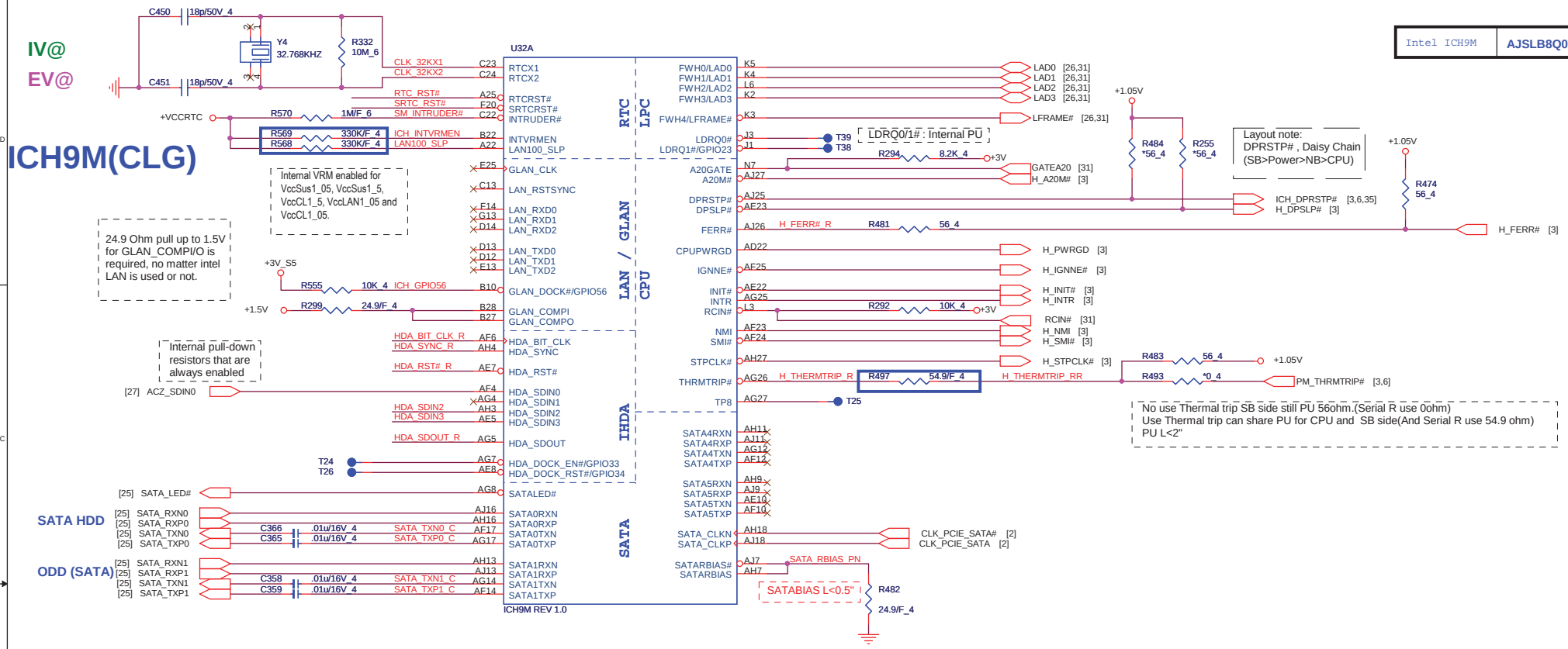
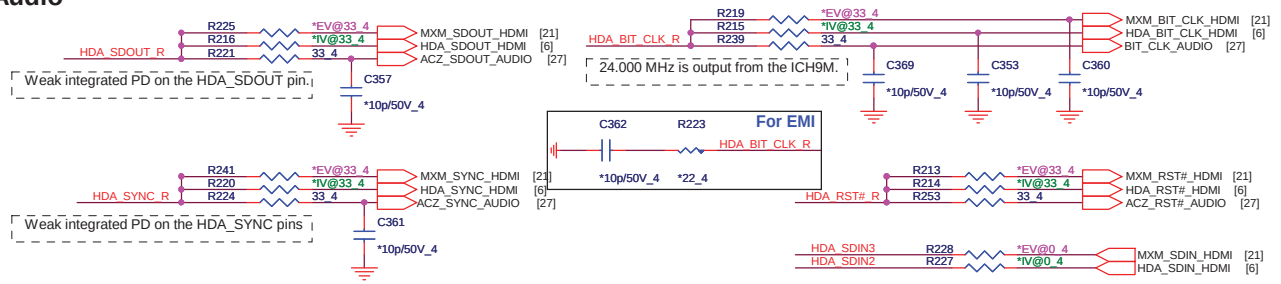
IV@

EV@

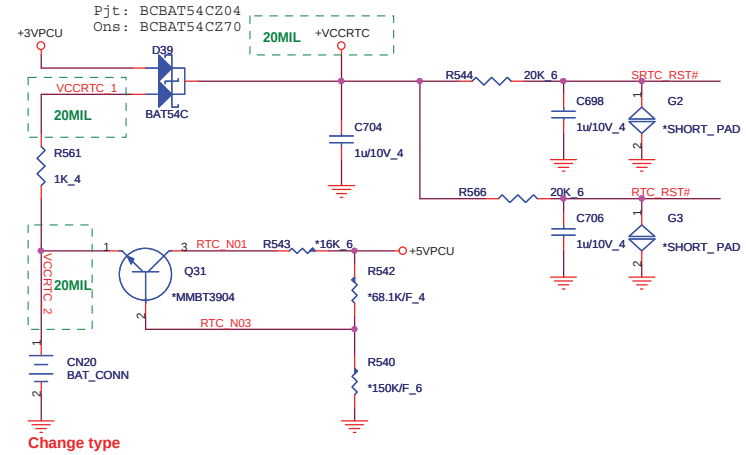
ICH9M(CLG)



HD Audio



RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT / Description 0 / 0 / RSVD 0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Set PCIE port config bit 1	[14] ICH_TP3 — ICH_TP3 — R545 — *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R240 — *1K_4 — +3V

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	ICH9M HOST	1A

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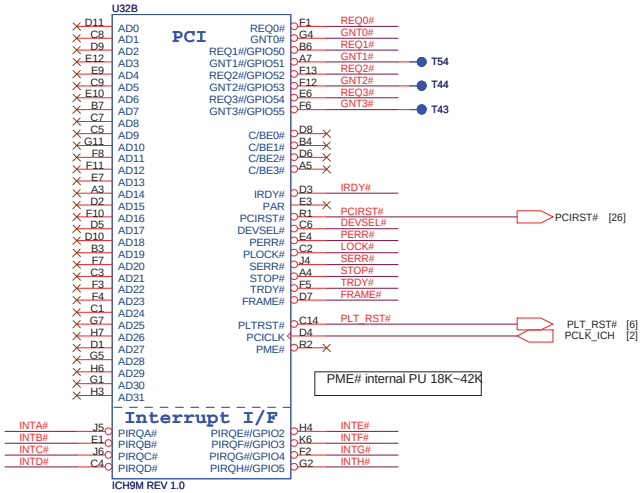
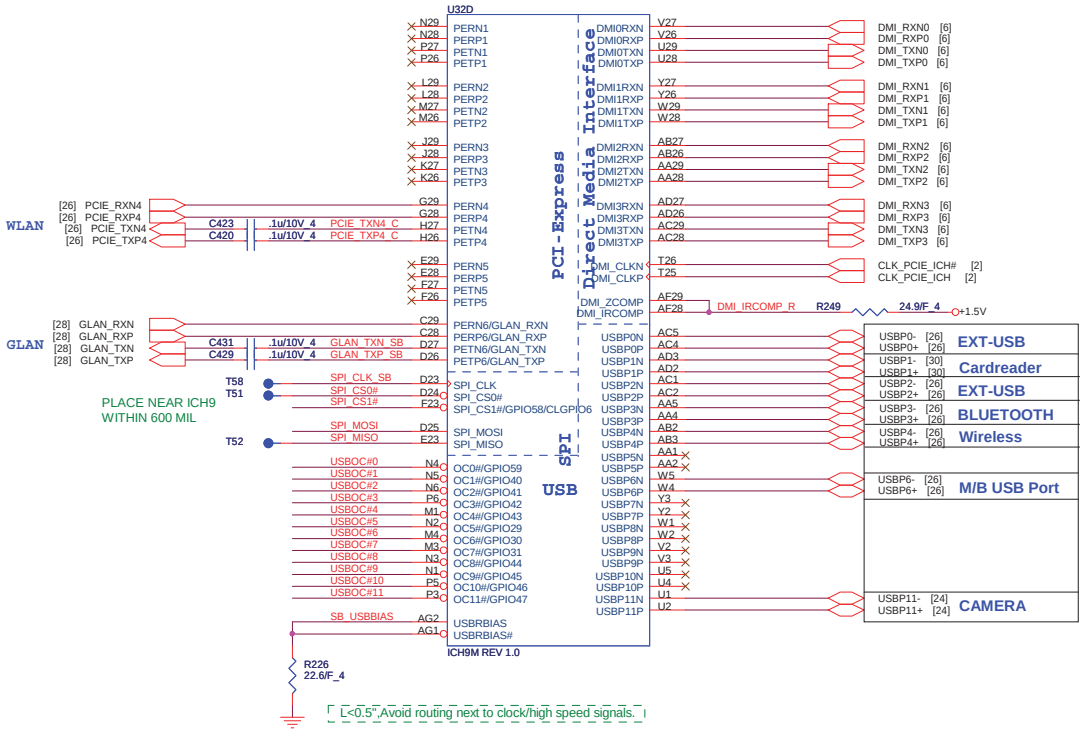
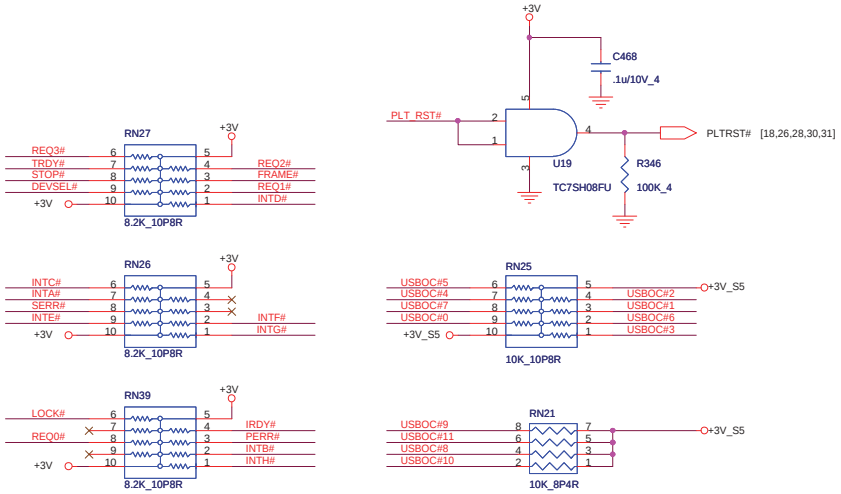
ICH9M(CLG)







South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R309 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R277 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R293 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / **LPC(Default)**	SPI_CS1# R274 *1K_4

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	ICH9M PCIE / PCI / USB	1A

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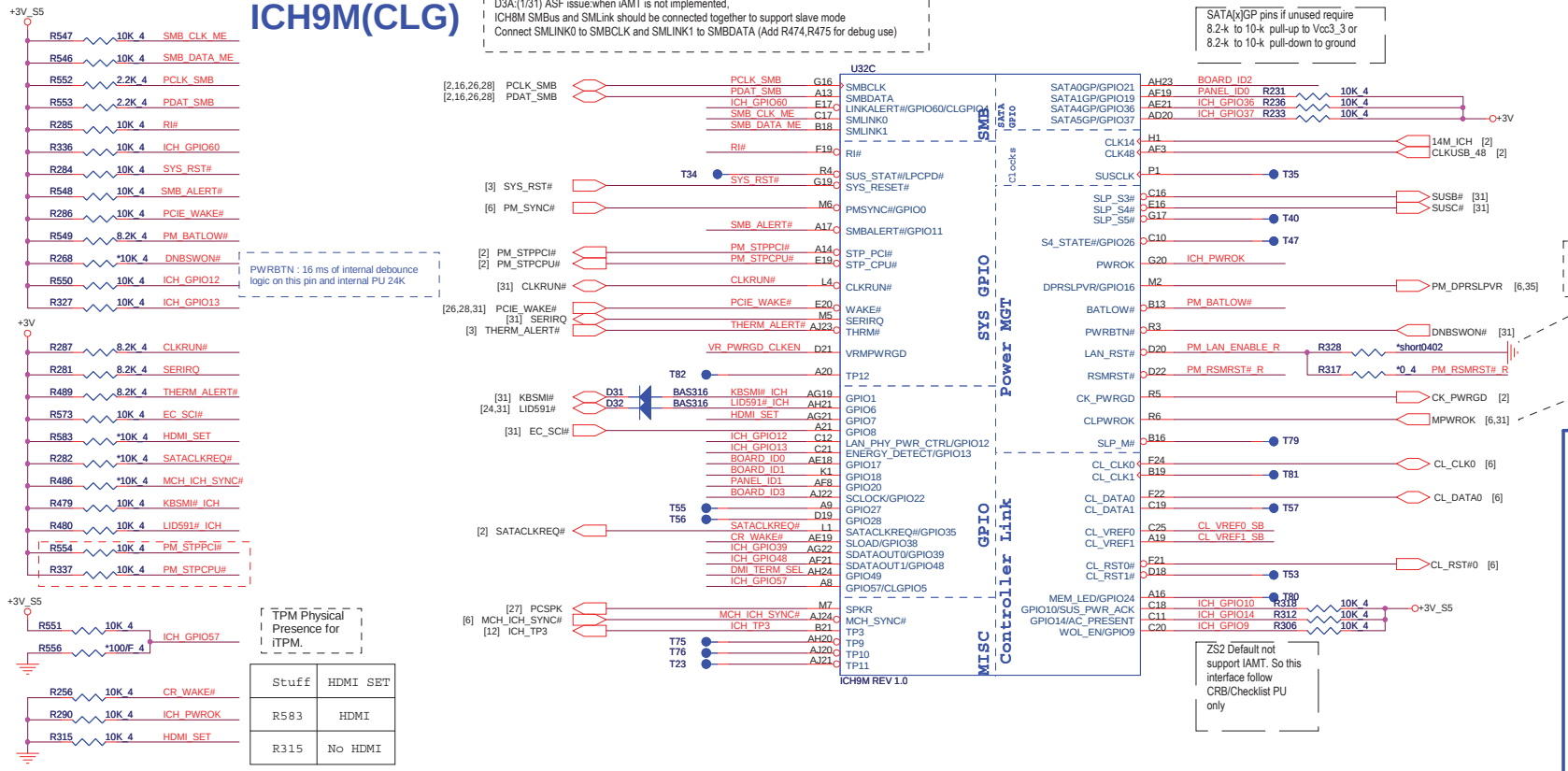
ICH9M(CLG)

D3A:(1/31) ASF issue:when iAMT is not implemented,
ICH8M SMBus and SMLink should be connected together to support slave mode
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

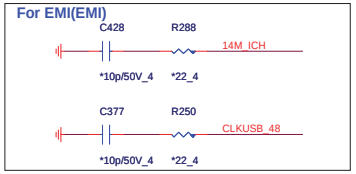
SATA[x]GP pins if unused require
8.2-k to 10-k pull-up to Vcc3_3 or
8.2-k to 10-k pull-down to ground



ZS2 Default not support IAMT. So this interface follow CRB/Checklist PU only

Stuff	HDMI SET
R583	HDMI
R315	No HDMI

For EMI(EMI)



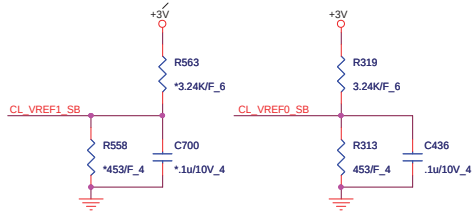
<Checklist ver0.8>
If integrated LAN is not used LAN_RST# tie it to GND.NC serial R from RSMRST#.
If Intel LAN is used with Wake On LAN, tie LAN_RST# to RSMRST# and NC 0ohm.

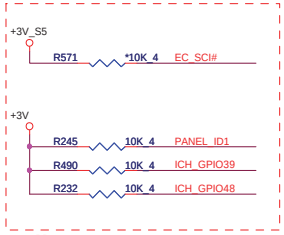
CL_PWROK must not assert after PWROK asserts for IAMT.
CL_PWROK to the NB and SB should be connected to existing PWROK inputs on the NB and SB on a platform with no IAMT

CL VREF

VREF1 CRB connect to +3V_S5
Checklist connect to +3V(iAMT reserve)

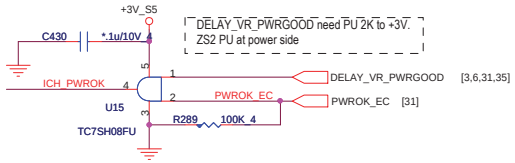
<Checklist ver0.8>
The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.





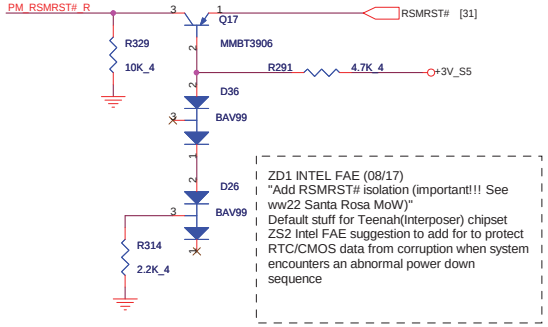
Follow CHECK LIST V1.5

ICH PWROK



DELAY_VR_PWRGOOD need PU 2K to +3V.
ZS2 PU at power side

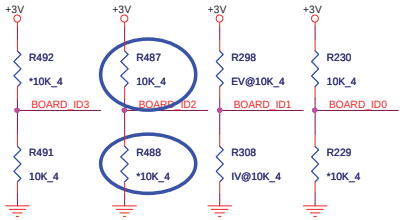
Resume RST



ZD1 INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"
Default stuff for Teenah(Interposer) chipset
ZS2 Intel FAE suggestion to add for to protect RTC/CMOS data from corruption when system encounters an abnormal power down sequence

M/B ID

ID0=0 -->ZK6 ,ID0=1 -->ZR6
ID1=0 -->UMA ,ID1=1 -->Discrete

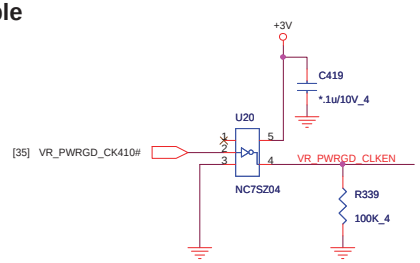


Board ID	ID3	ID2	ID1	ID0
A-SMT,ID1=0 -->UMA ,ID1=1 -->Discrete	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R271 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R485 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	ICH9M GPIO	1A

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ICH9M(CLG)

IV@
EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF

2~3.456v 3.6uA_G3

5V 2mA

5V S0:2mA S3/4/5:1mA

MODIFY

330 Ohms@ 100 MHz , 0805

1.5V 646mA

1.5V 47mA

VCC1_5_A 1.5V 1342mA

1.5V 11mA

1.05V , Powered by VCC1_05 in S0

3.3V S0:19mA S3/4/5:78mA

If use SB MAC for LAN function. And support wake up need connect to relation power.

1.5V 23mA

1.5V 80mA

MODIFY

3.3V 1mA

1.05V 1634mA

1.5V 23mA

500 mA, 20%

1.05V 48mA

5 Ohms @ 100 MHz , 0.7A

1.05V 2mA

3.3V 308mA

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

1.5V / 3.3V 11mA

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

1.5V / 3.3V S0:11mA S3/4/5:1mA

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5
VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

3.3V S0:212mA S3/4/5:53mA

VCCCL1_05 power by VCC1_05_A in S0
VCCCL1_5 power by VCC1_5_A in S0

3.3V S0:19mA S3/4/5:73mA

If use SB MAC for LAN function. And support wake up need connect to relation power.

U32F — ICH9M REV 1.0

U32E — ICH9M REV 1.0

Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	ICH9 POWER	1A

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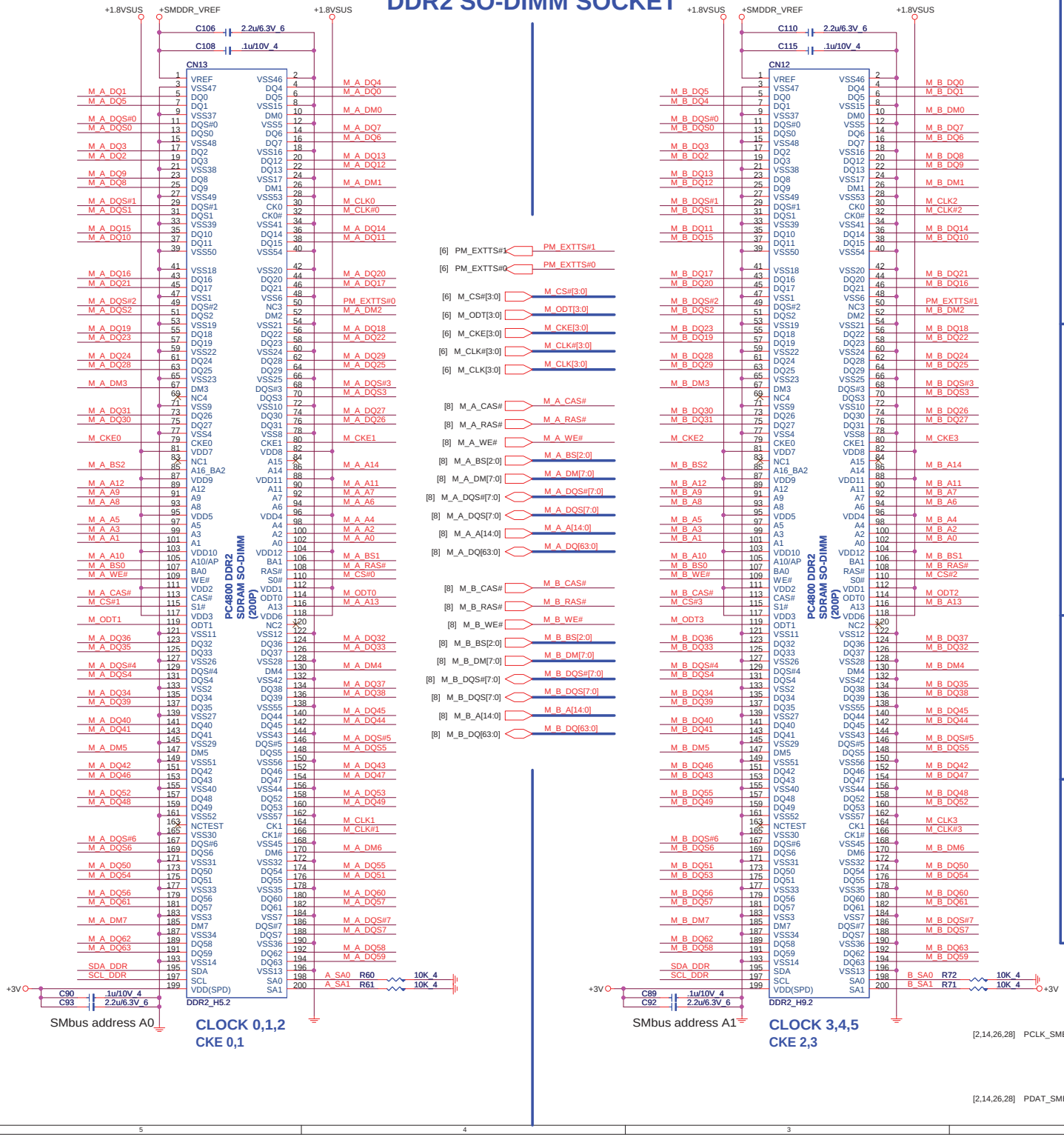
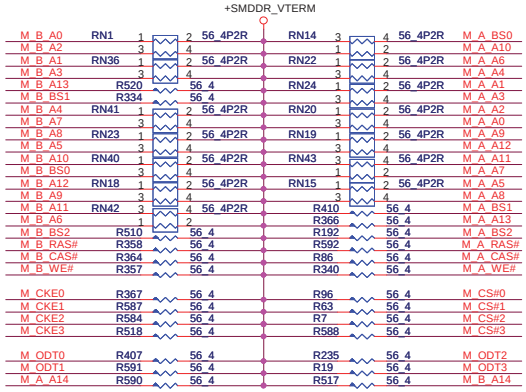
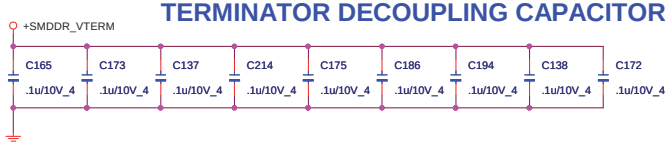
DDR2 SO-DIMM SOCKET



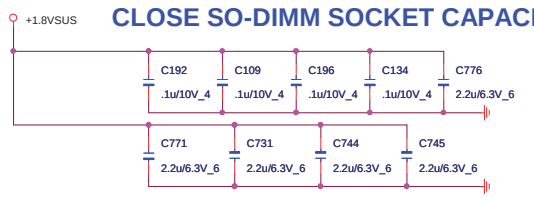
DDR2 TERMINATOR



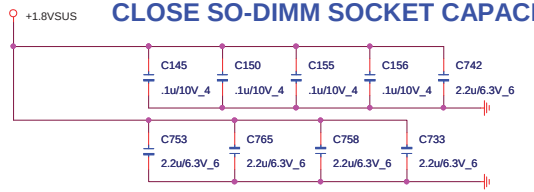
TERMINATOR DECOUPLING CAPACITOR

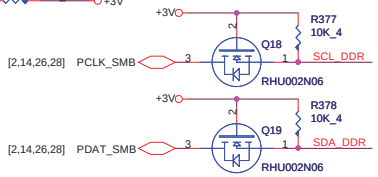


CLOSE SO-DIMM SOCKET CAPACITORS



CLOSE SO-DIMM SOCKET CAPACITORS





Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	DDRII SO-DIMM	1A

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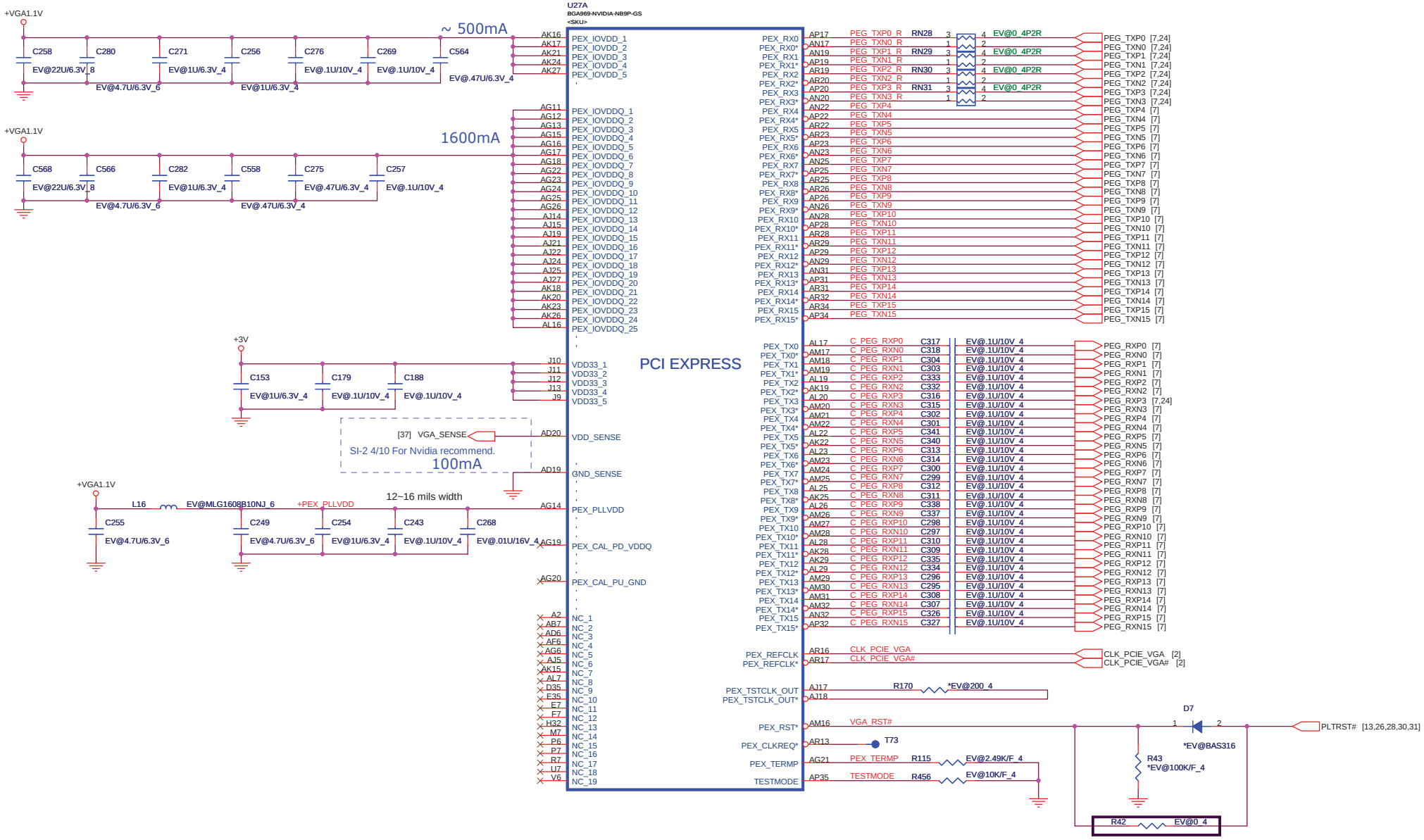
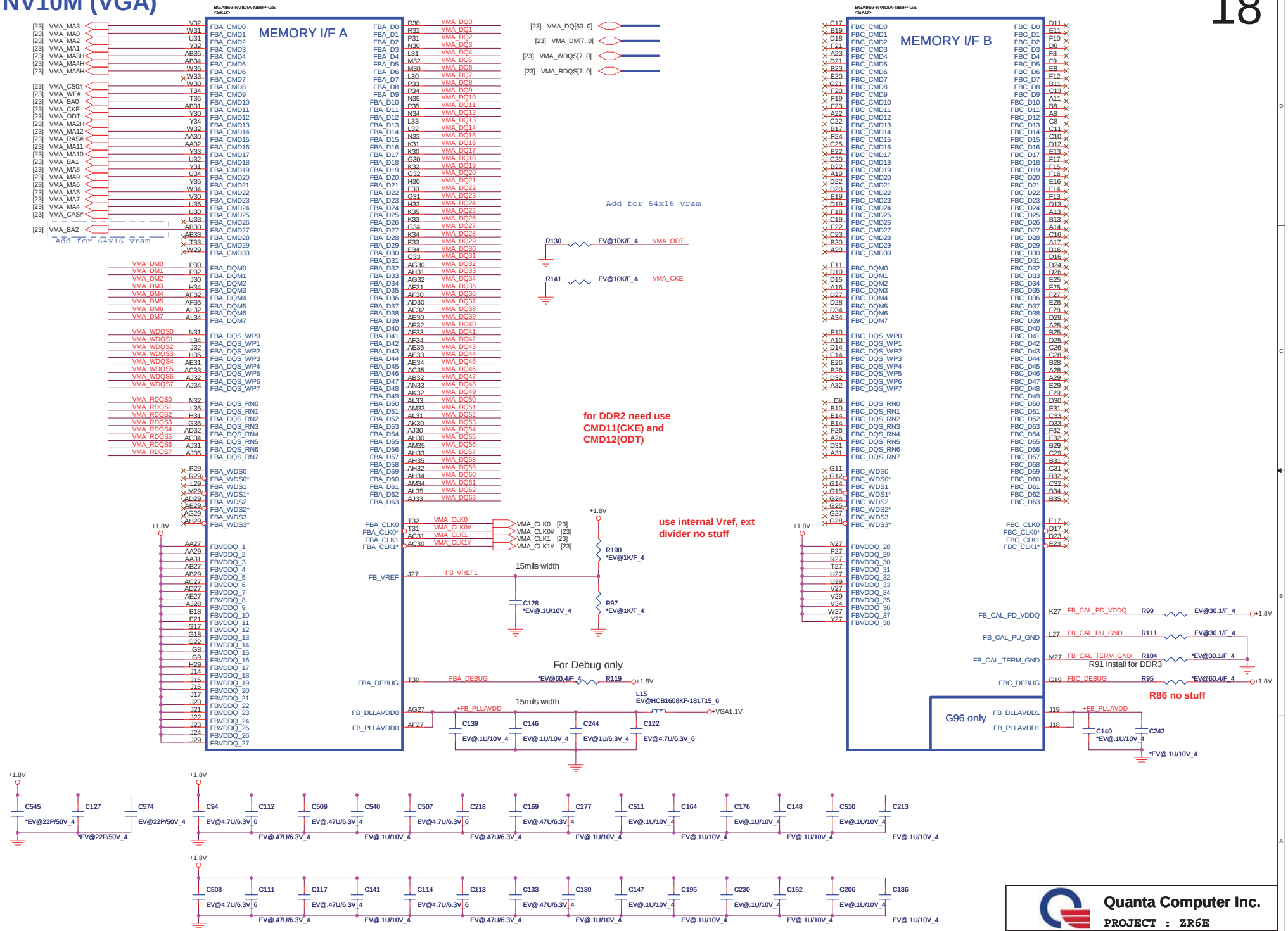
NV10M (VGA)



Quanta Computer Inc.			
PROJECT : ZR6E			
Size	Document Number		Rev
	NV10X (PCIE I/F) 1/5		1A
Date: Tuesday, May 19, 2009	Sheet 17 of 39		

NV10M (VGA)



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	NV10X (MEMORY I/F) 2/5	1A

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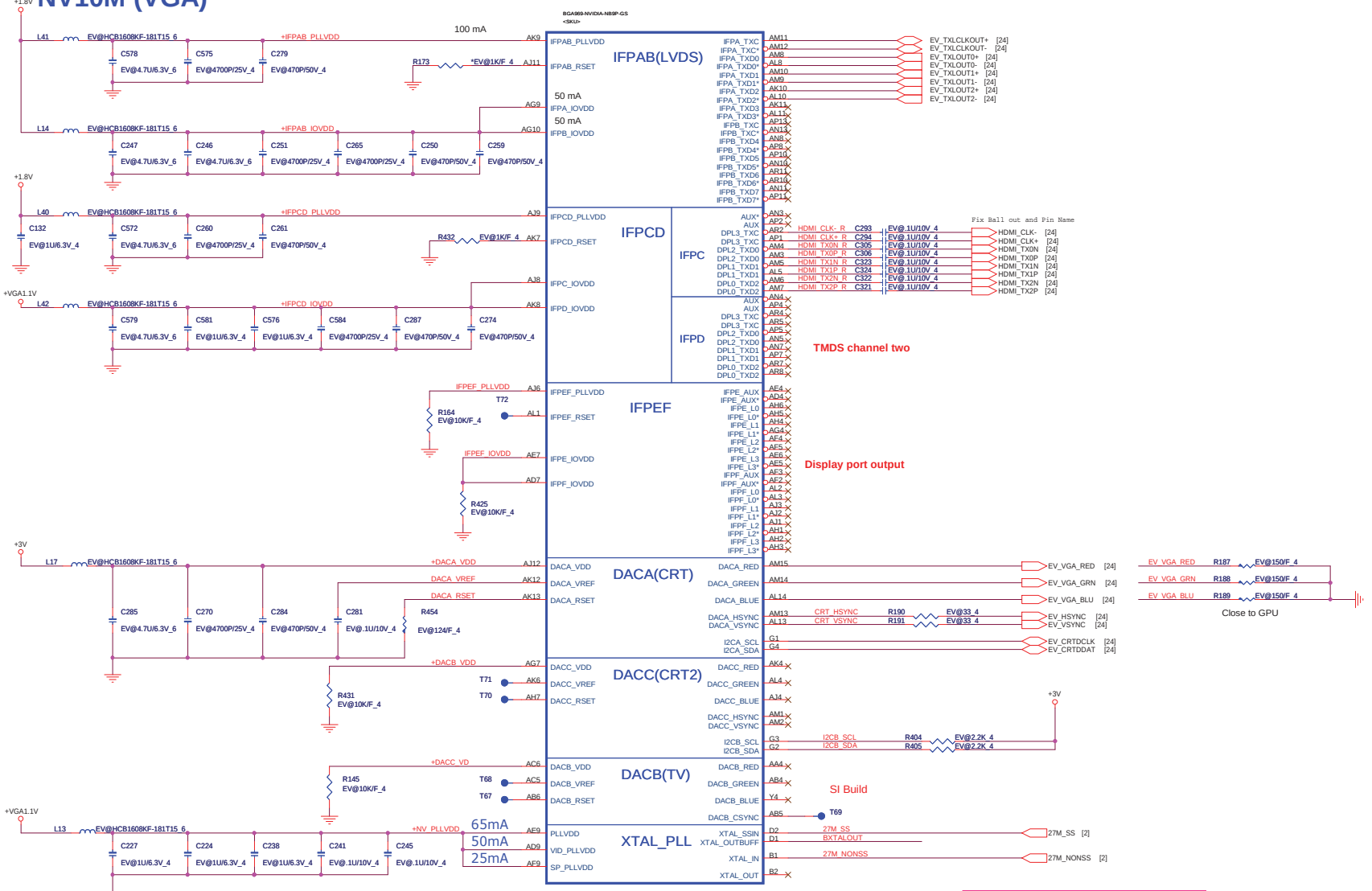
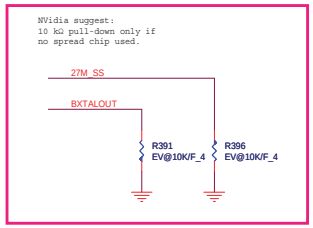
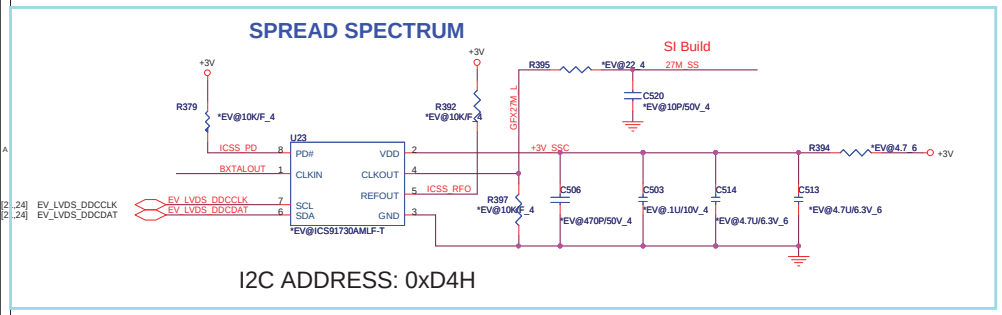
NV10M (VGA)





SPREAD SPECTRUM



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	NV10X (DISPLAY) 3/5	1A

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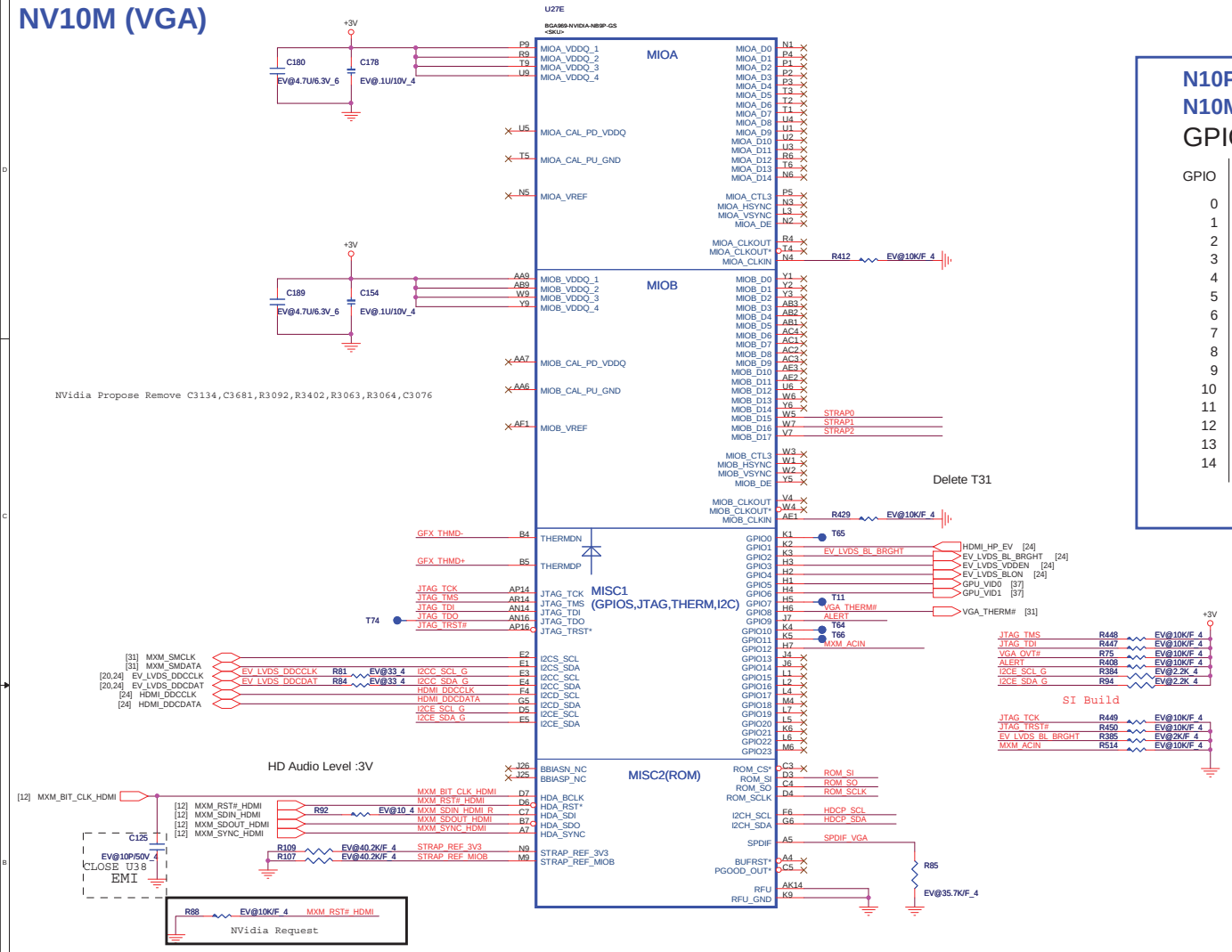
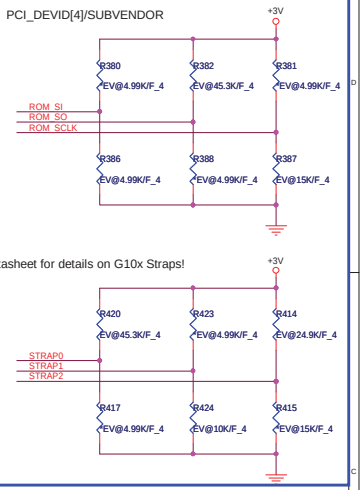
NV10M (VGA)



N10P-GE1 (G96) Straps
N10M-GE1 (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



PCI_DEVID: STRAP2

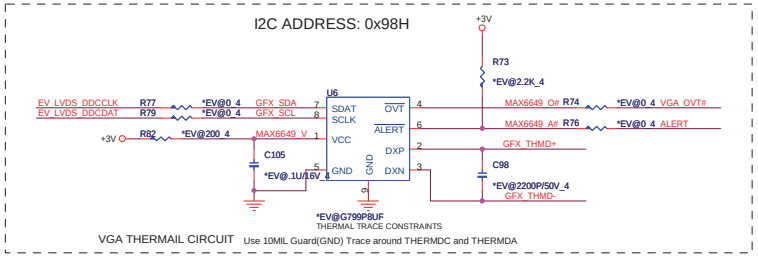
NB9M-GE	0x06E	8	1000
NB9M-GS	0x06E	9	1001
NB9P-GE2	0x064	8	1000
NB9P-GS	0x064	9	1001
N10P-GE1	0x065	2	0010
N10M-GE1	0x06E	C	1100 default

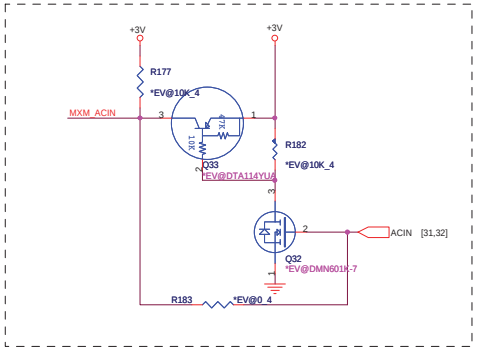
Logical Strap Bit Mapping

R414	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

R386	Config	Definitions	Die
CS25102FB02 5K	64Mx16 DDR2	Hynix	E
CS31002FB26 10K	64Mx16 DDR2	Samsung	Q
CS32002FB29 20K	64Mx16 DDR2	Samsung	E

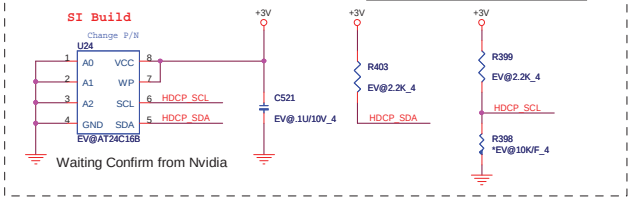
I2C ADDRESS: 0x98H





HDCP ROM

DHCP ROM	
HDCP_SCL	Low: Crypto ROM **Hi: I2C ROM**



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	NV10X (GPIO & STRRAPS) 4/5	1A

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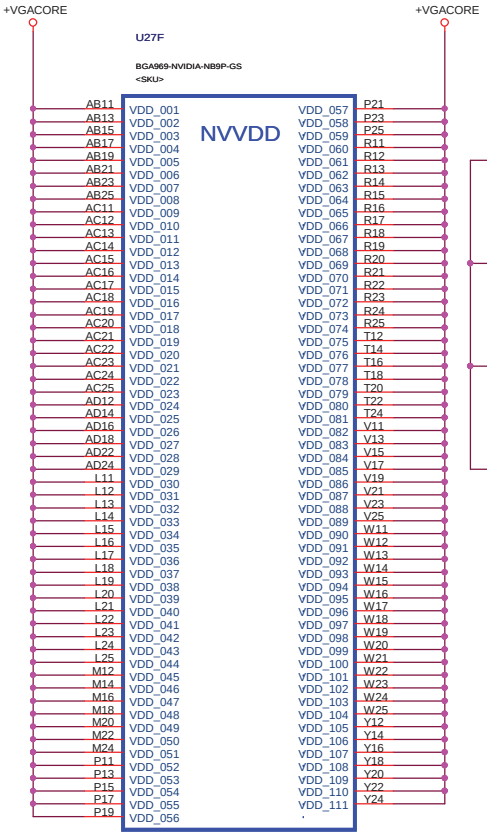
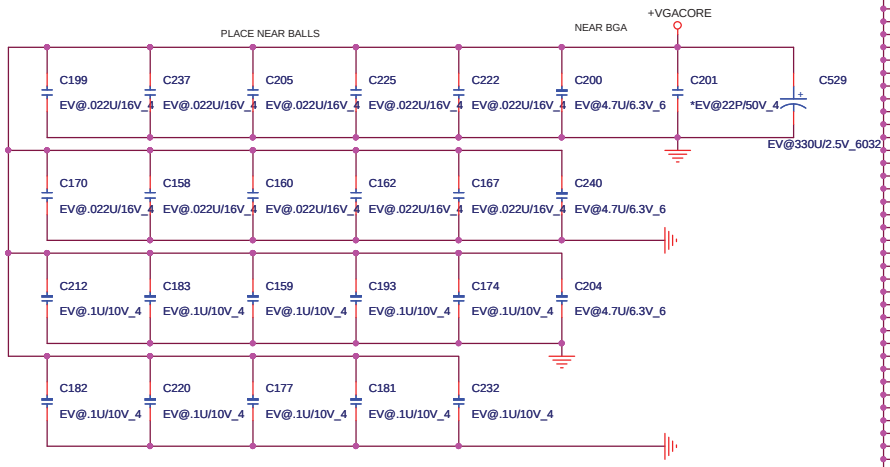
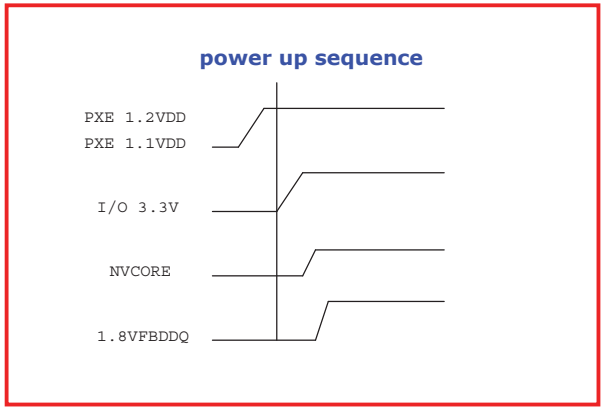
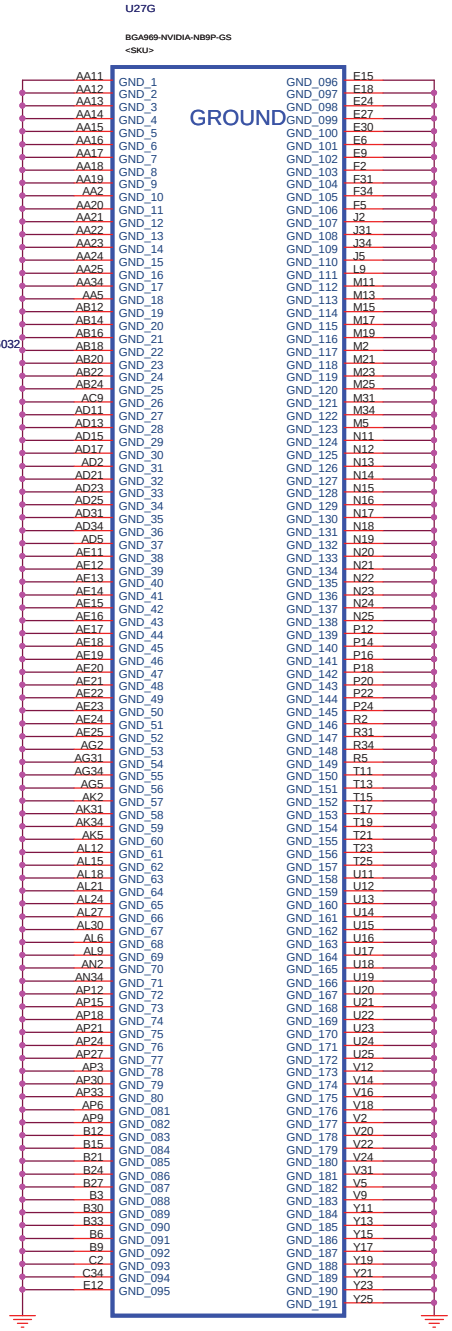
NVVDD Decoupling



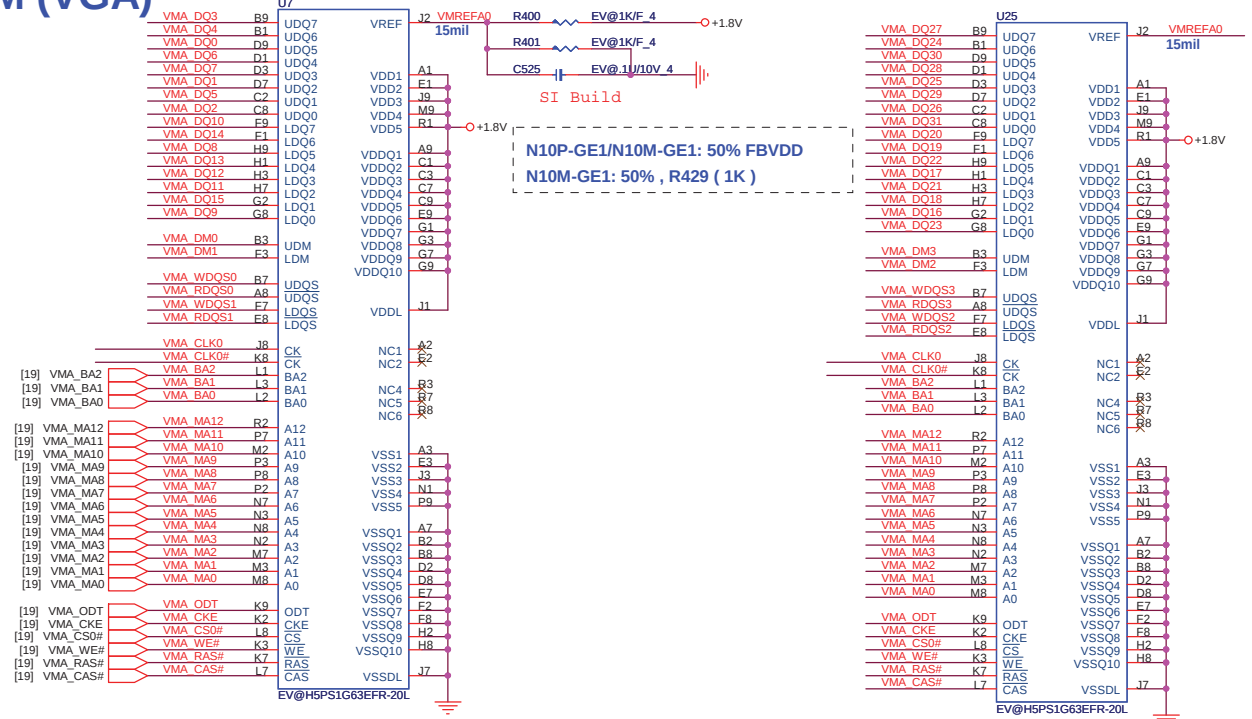


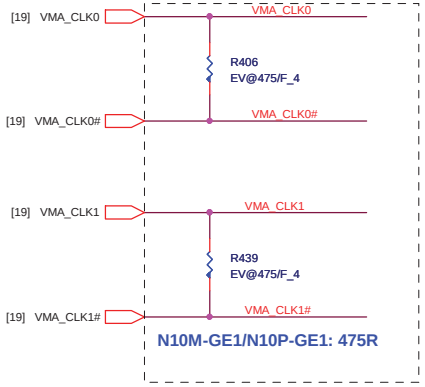
Follow Design Guide DG-03276-001 4.7uFx3 and 0.22x10 uF instead of 0.1uF x10





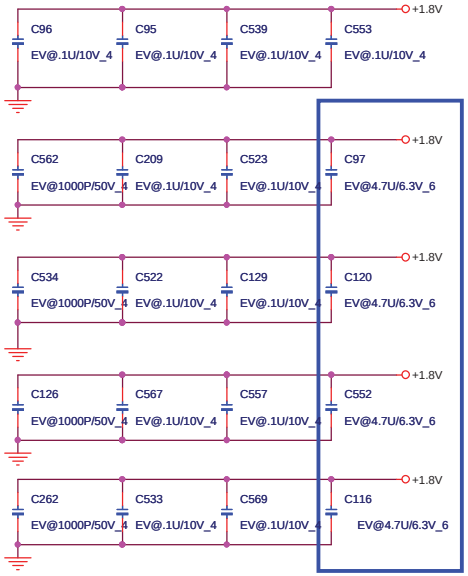
NV10M (VGA)

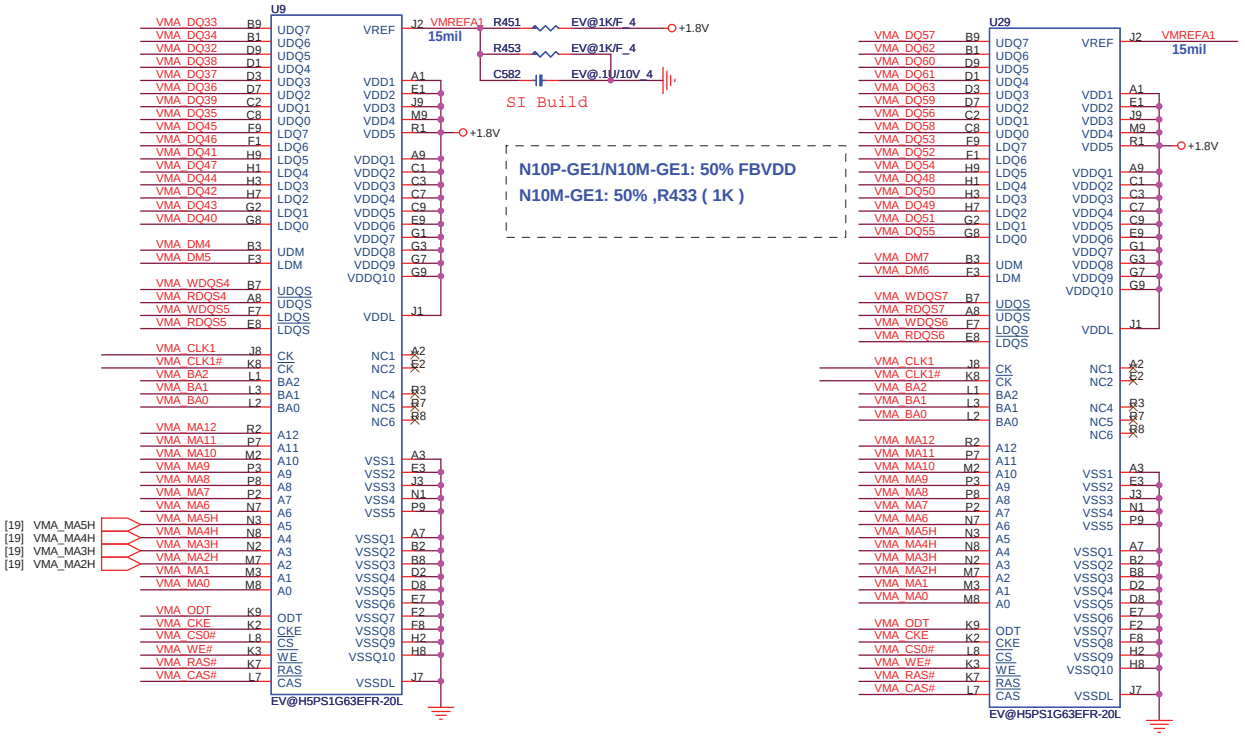




CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

(By pass capacitor)





[19] VMA_DQ[63..0]
[19] VMA_DM[7..0]
[19] VMA_WDQS[7..0]
[19] VMA_RDQS[7..0]

For DB:
N10P/N10M : AKD5LG-T510(Samsung,64M*16)
AKD5LG-TW02(Hynix,64M*16)

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	NV10X VRAM-1(GDDR2 BGA84)	1A

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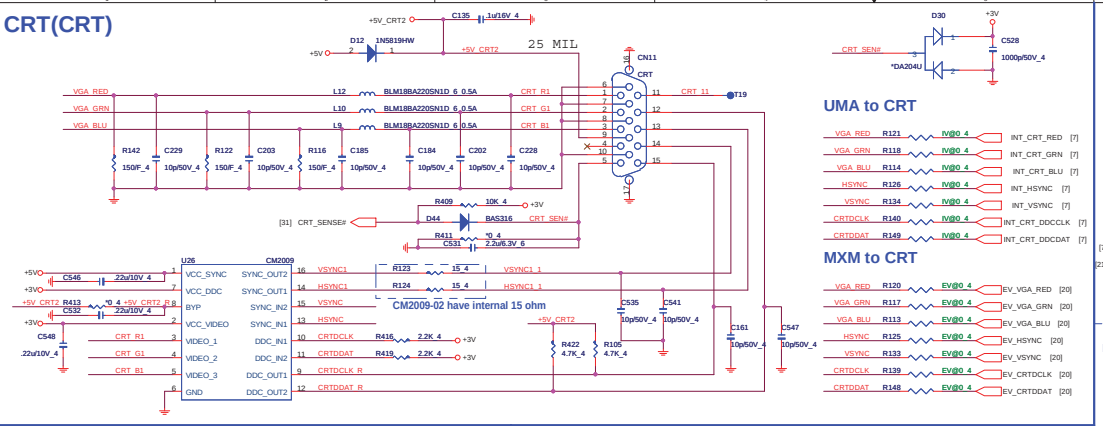
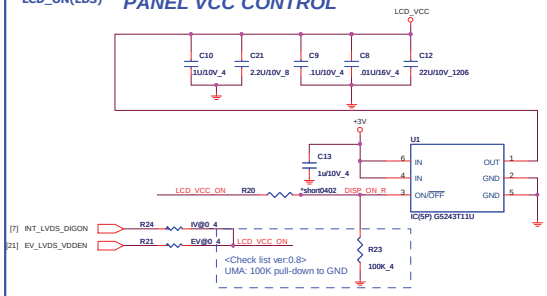
CRT(CRT)



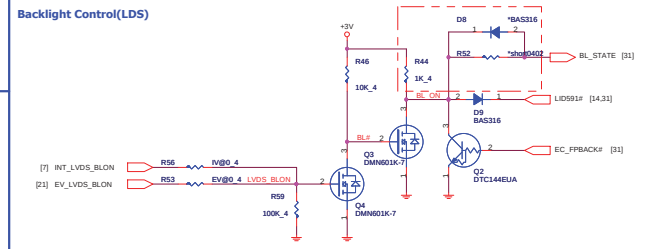
UMA to CRT

MXM to CRT

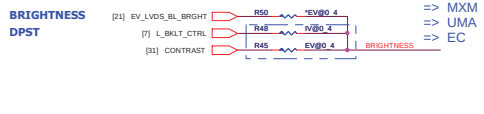
LCD_ON(LDS) PANEL VCC CONTROL



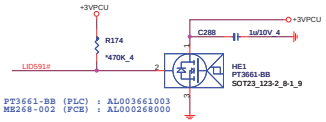
Backlight Control(LDS)



LVDS(LDS)



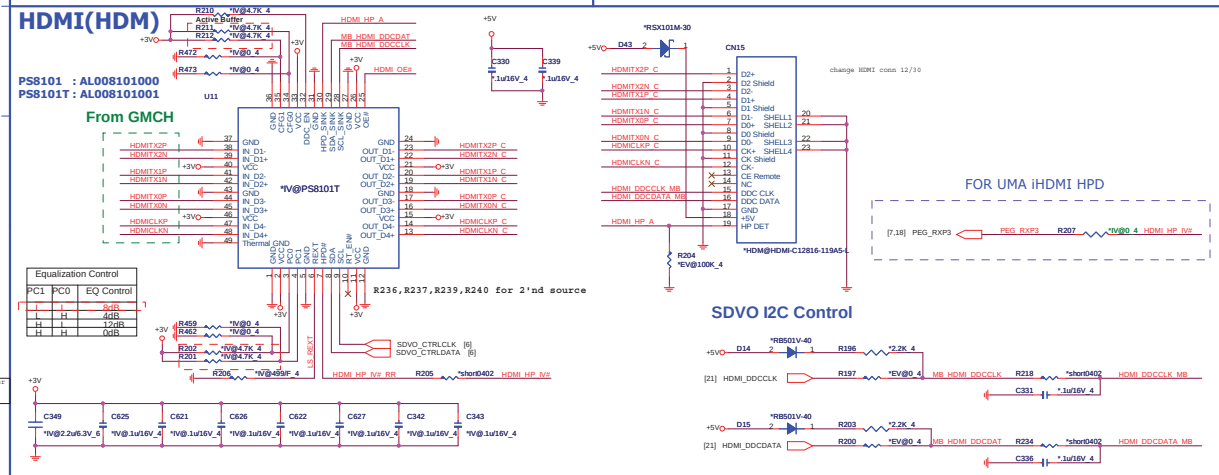
Lid Switch (HSR)



LCD EDID SMBus PU

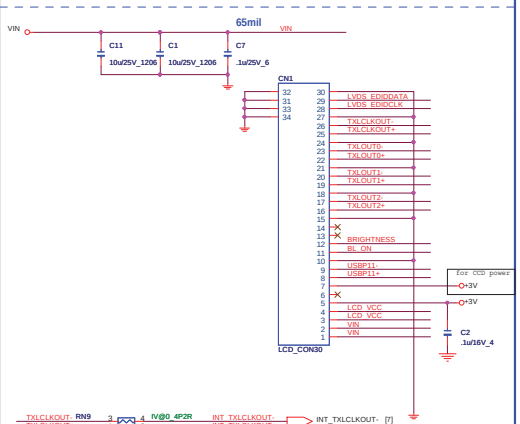
HDMI(HDM)

PS8101 : AL008101000
PS8101T : AL008101001

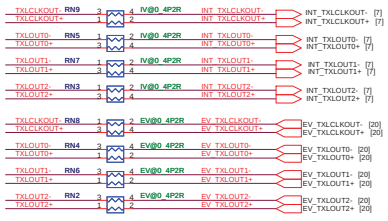


SDVO I2C Control

LVDS(LDS)

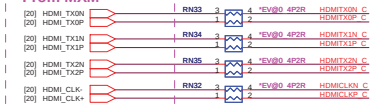


UMA to LVDS

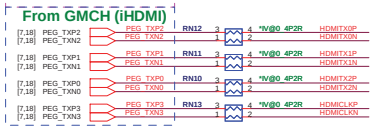


MXM to LVDS

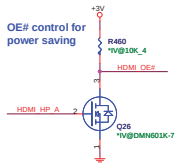
From MXM



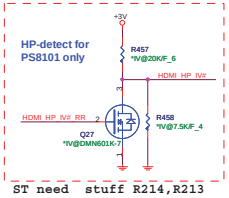
From GMCH (iHDMI)



OE# control for power saving

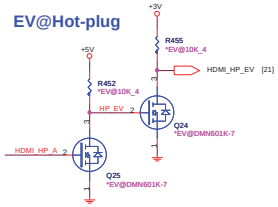


HP-detect for PS8101 only



ST need stuff R214,R213

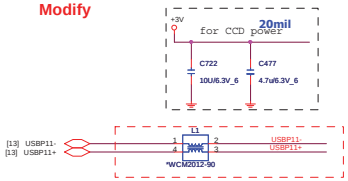
EV@Hot-plug



FOR NV HDMI

NV suggestion near HDMI connector

Camera(CCD) Modify



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	LVDS/CRT/CCD/HDMI/MIC	1A

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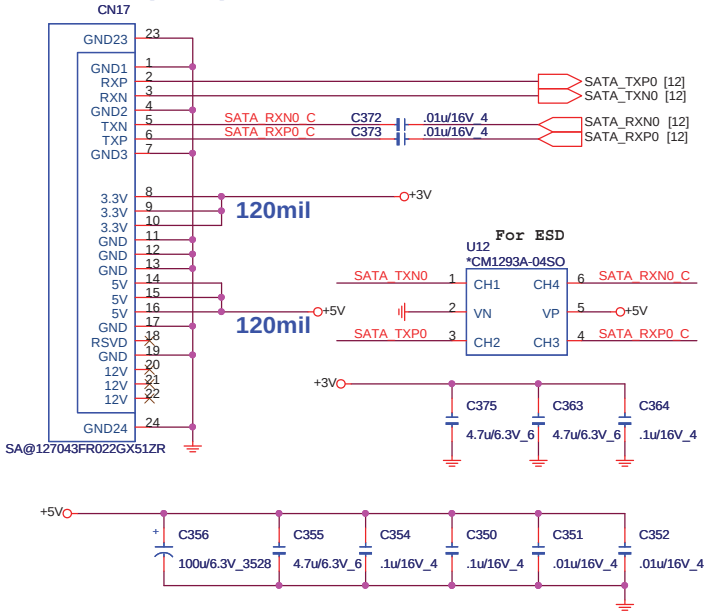
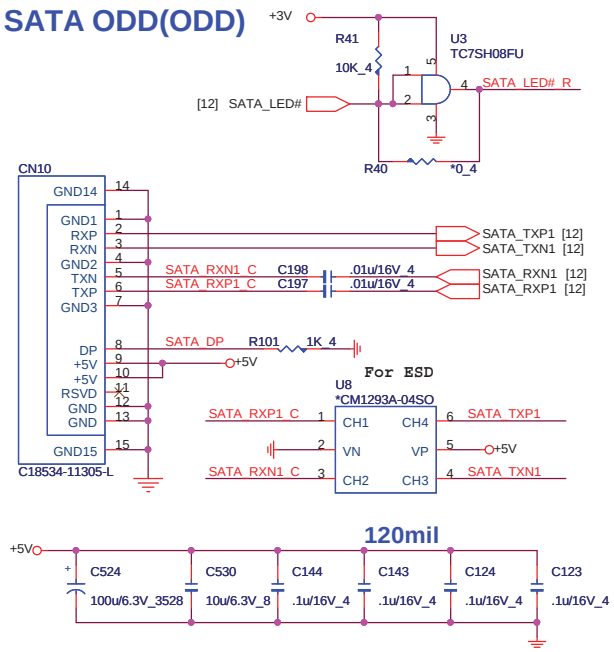
SATA HDD(HDD)

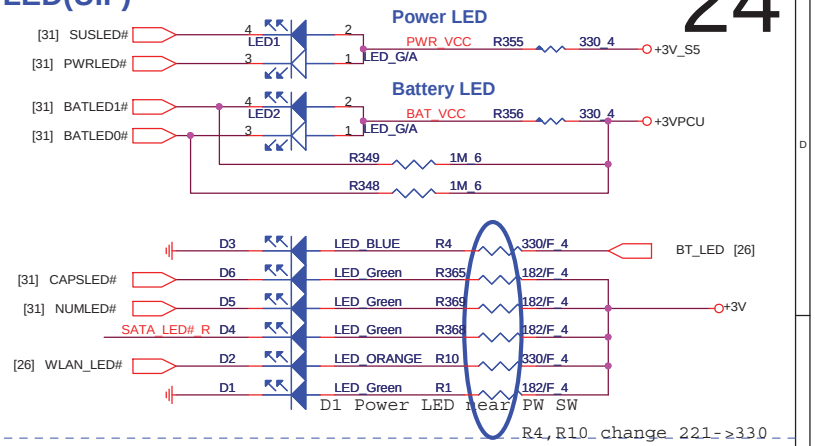


SATA ODD(ODD)



LED(UIF)

Power/Suspend: Green/Amber

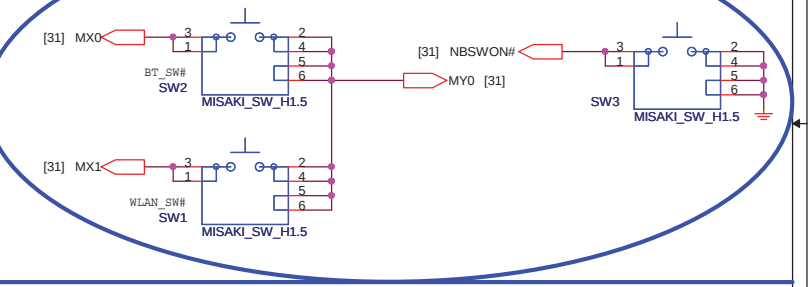


R4,R10 change 221->330

R1,R365,R368,R369 change 221->182

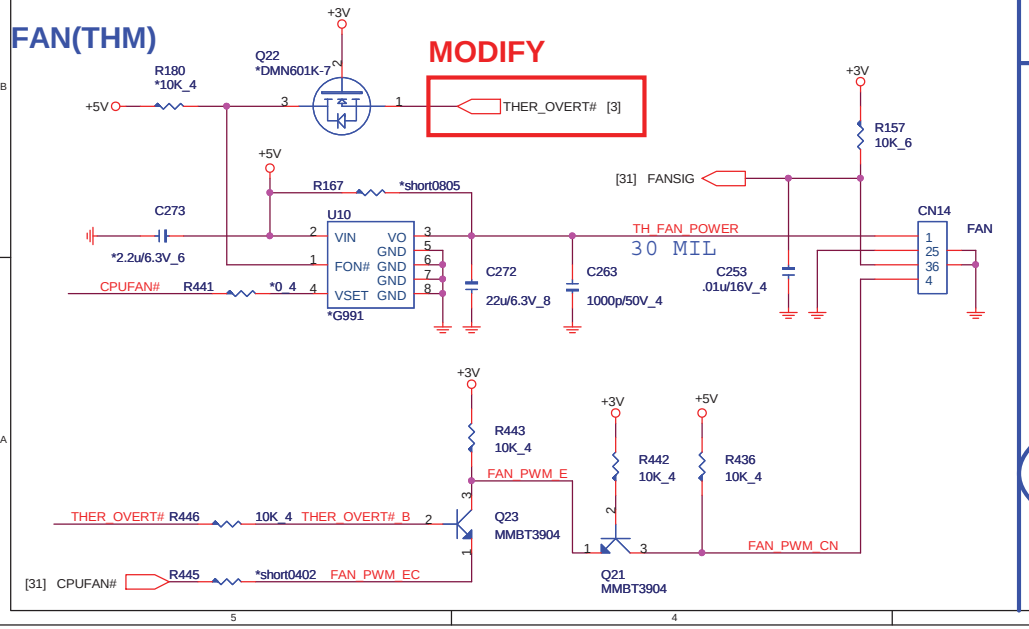
Power Button (UIF)

SW1,SW2,SW3 change P/N to DHP00BA1G04



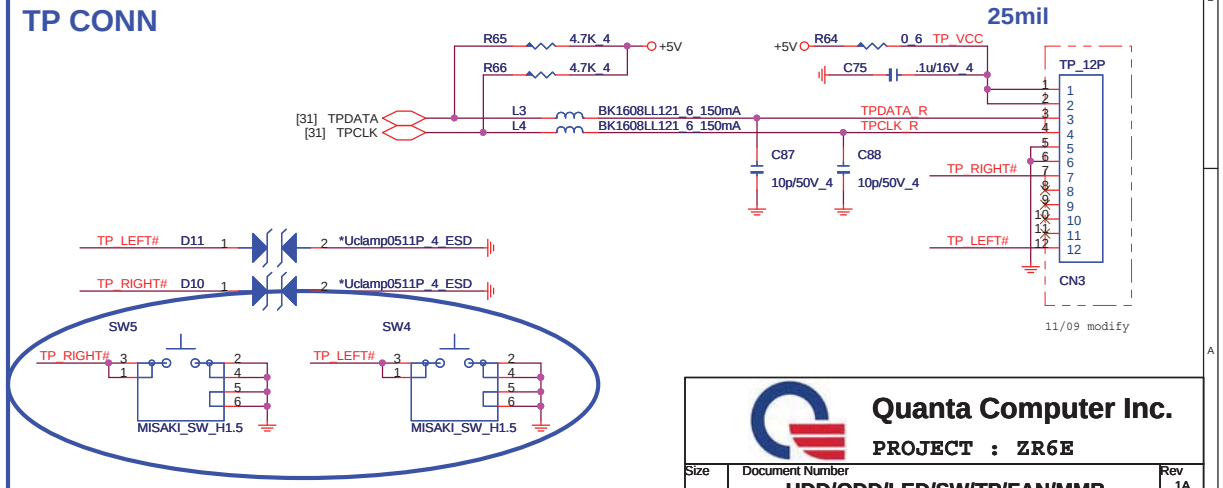
FAN(THM)

MODIFY



TP CONN

25mil



11/09 modify

SW4,SW5 change P/N to DHP00BA1G04

Quanta Computer Inc.

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Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN/MMB	1A

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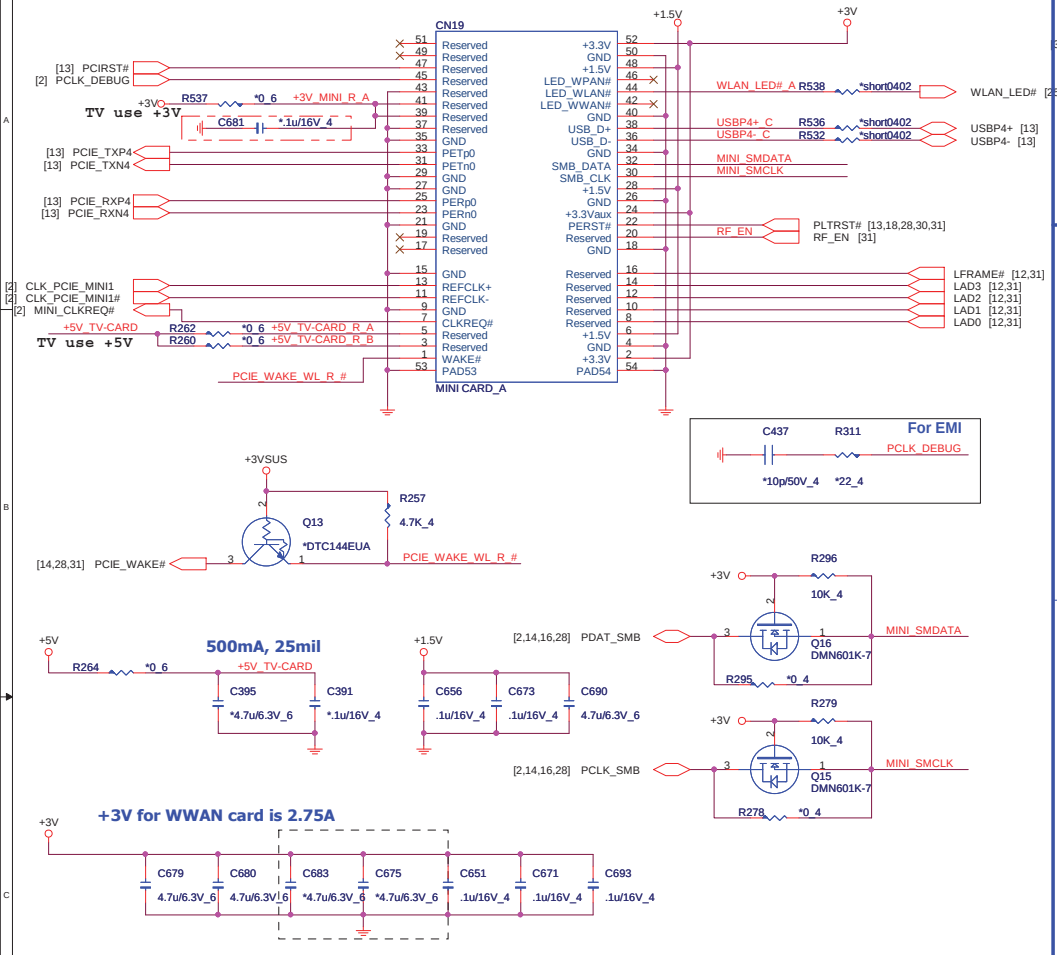
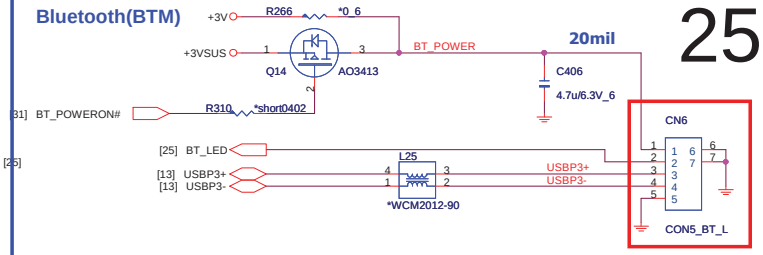
MINI-CARD(MPC)

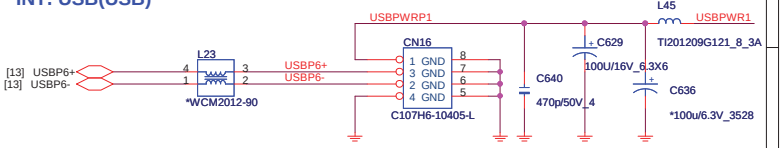


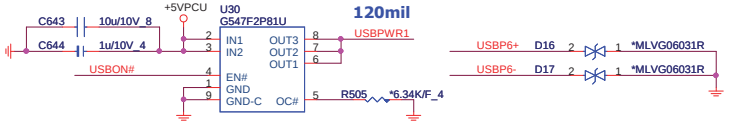
Bluetooth(BTM)



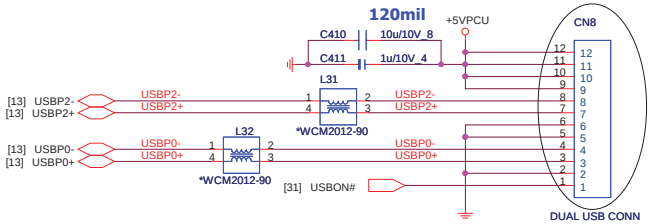
MODIFY Follow Z07

INT. USB(USB)



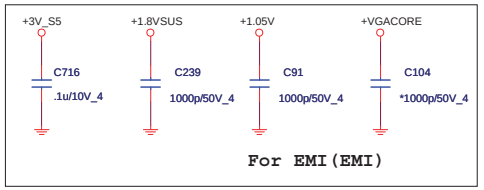


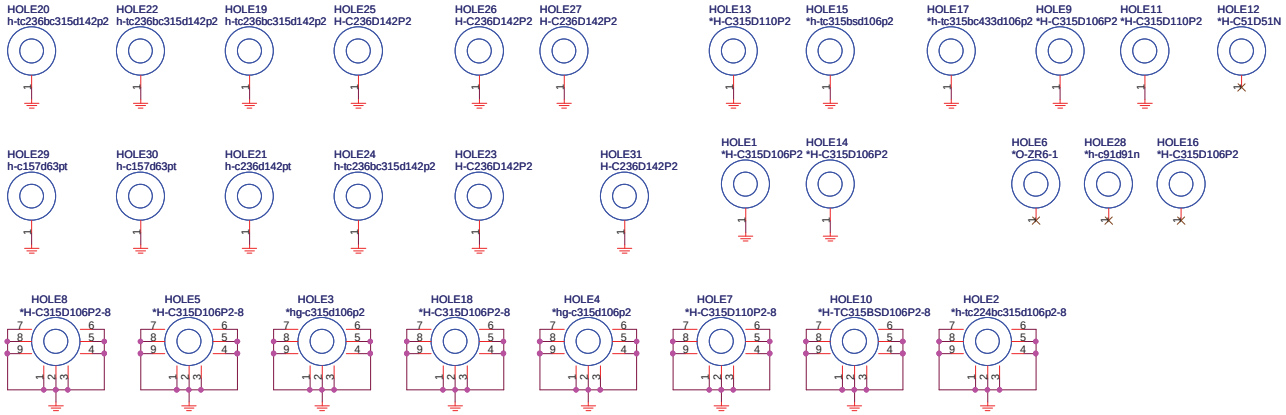
EXT. USB(USB)



Modfiy C

(OTH)





Quanta Computer Inc.

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Size	Document Number	Rev
	MINI/USB/BT/HOLE	1A

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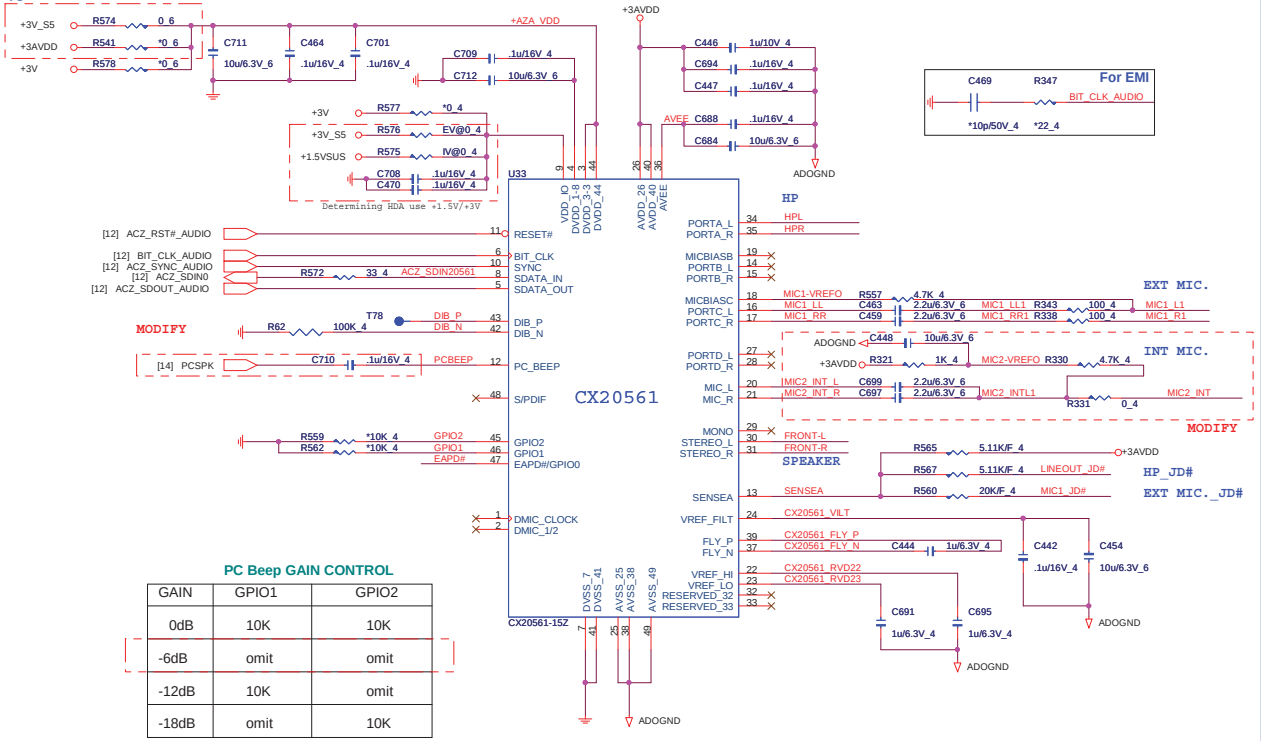
Codec CX20561-15Z (ADO)

QFN

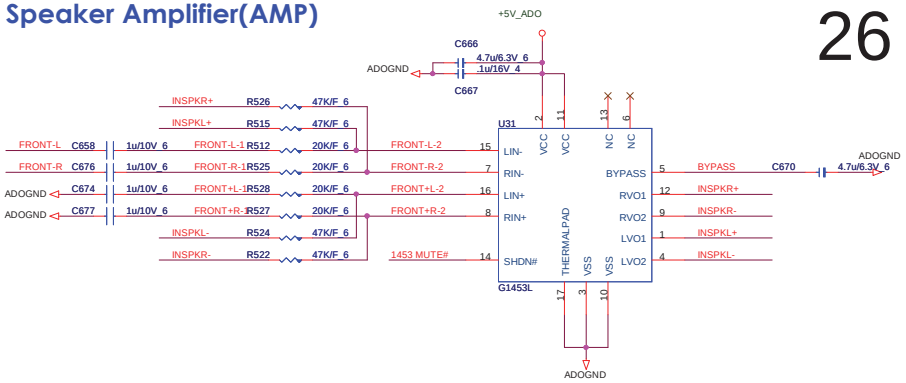
MODIFY REV:C



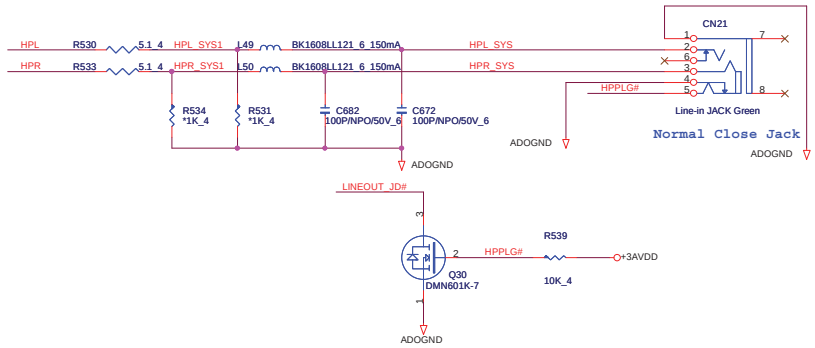
PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

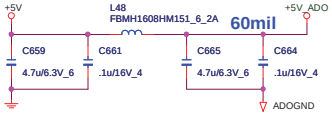
Speaker Amplifier(AMP)



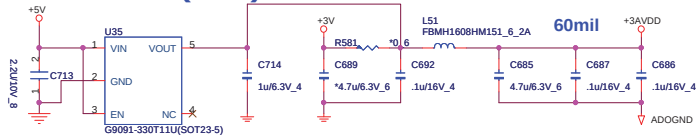
LINE OUT(AMP)



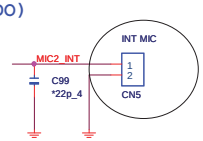
AMP Power(AMP)



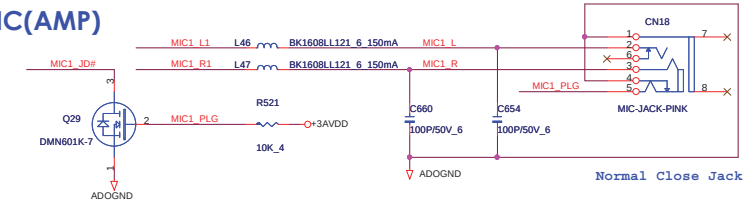
CODER Power(ADO)



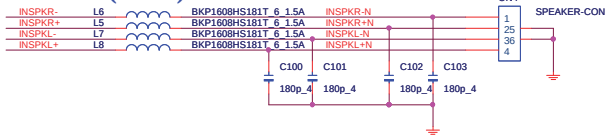
INT MIC.(ADO)



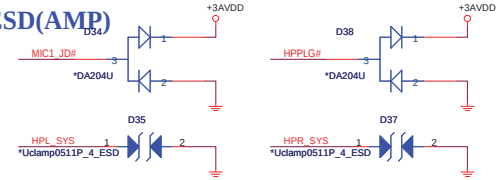
MIC(AMP)



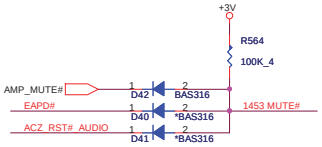
SPEAKER(AMP)



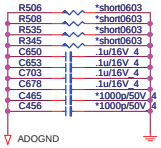
ESD(AMP)



MUTE(AMP)



(ADO)



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	CODEC/AMP/MDC	1A

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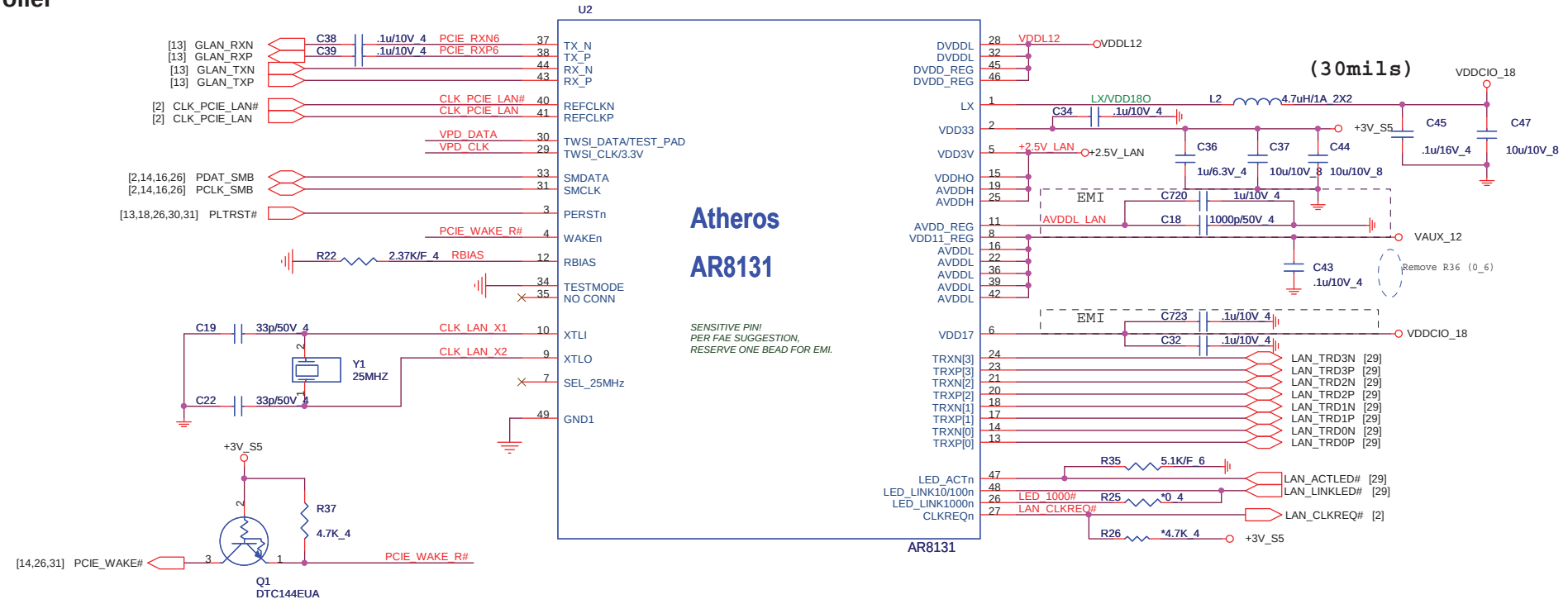
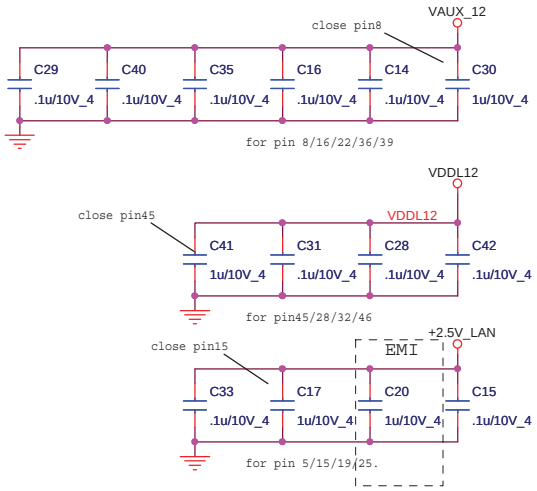
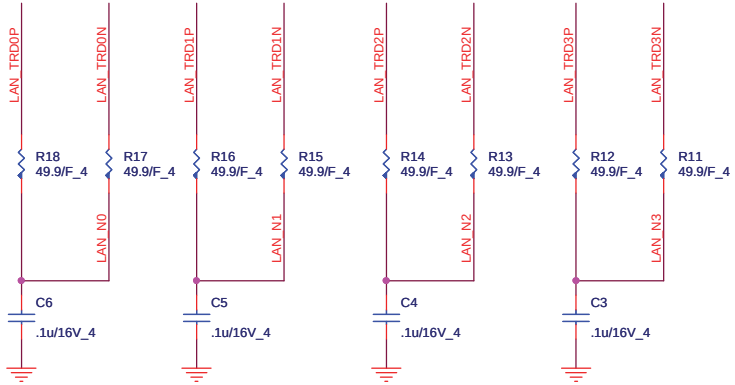
LAN Controller



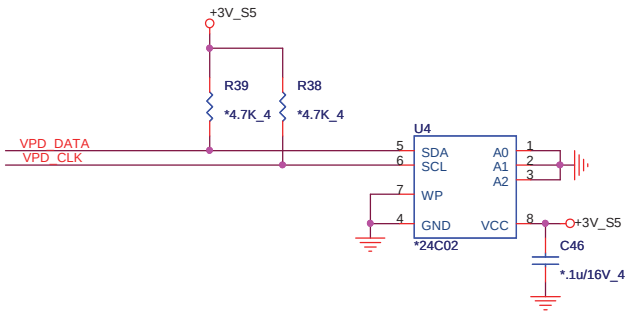
Decoupling CAP



PLACE NEAR IC SIDE



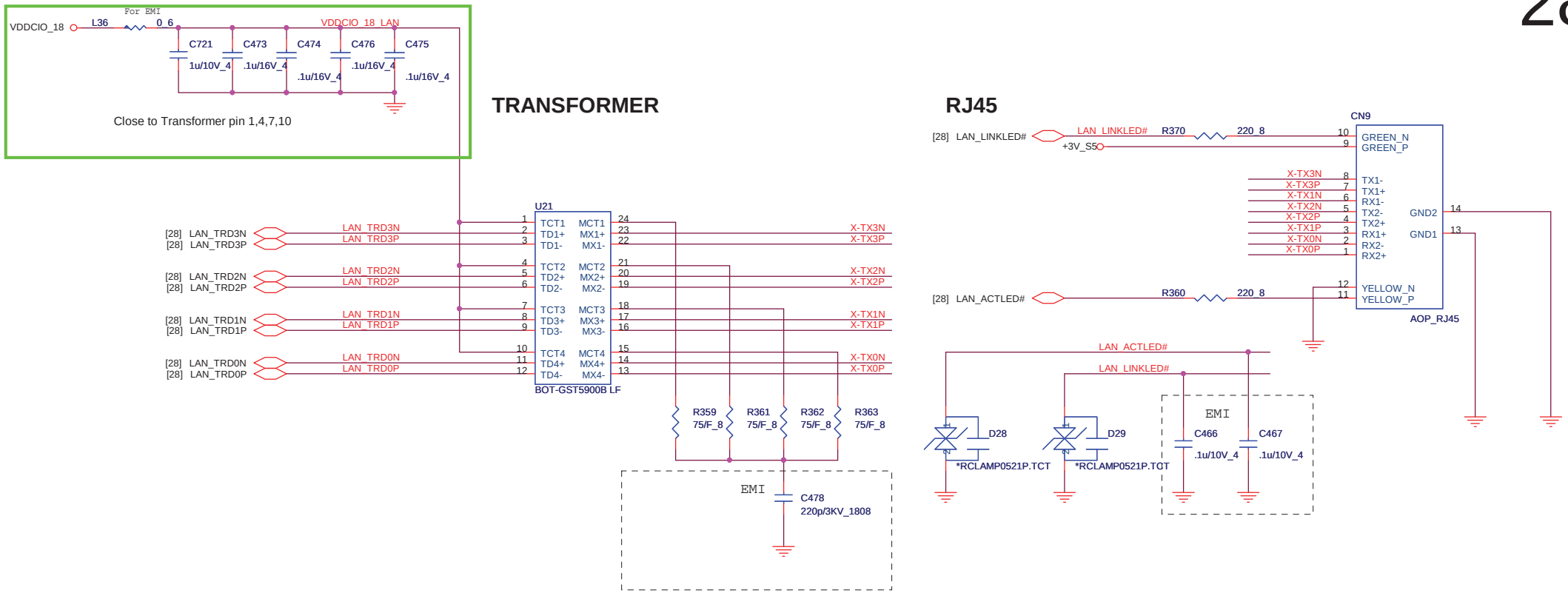
EEPROM



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	AR8131 GLAN	1A
Date: Tuesday, May 19, 2009	Sheet 27 of 39	



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	LAN Transformer and RJ45/BT	1A

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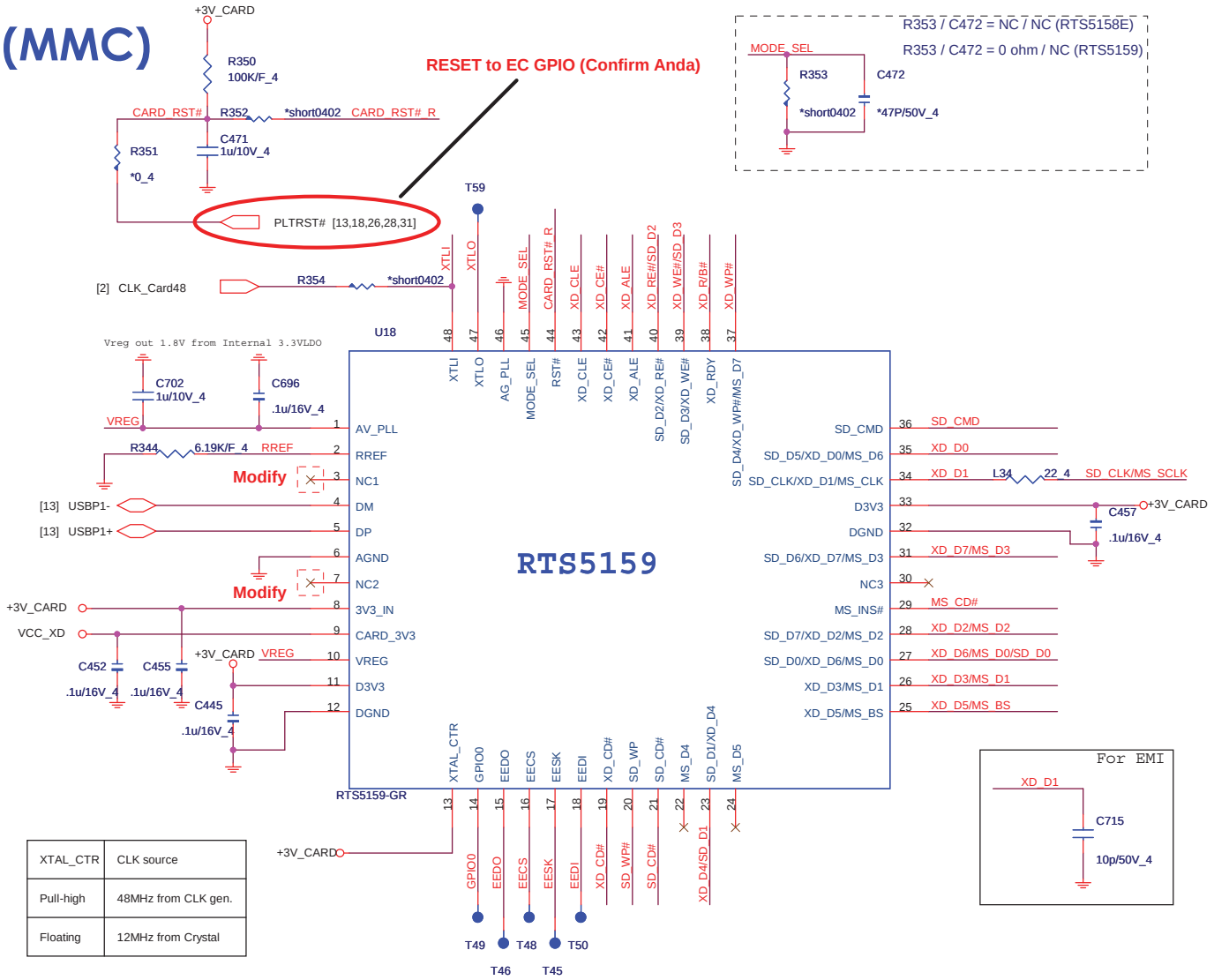
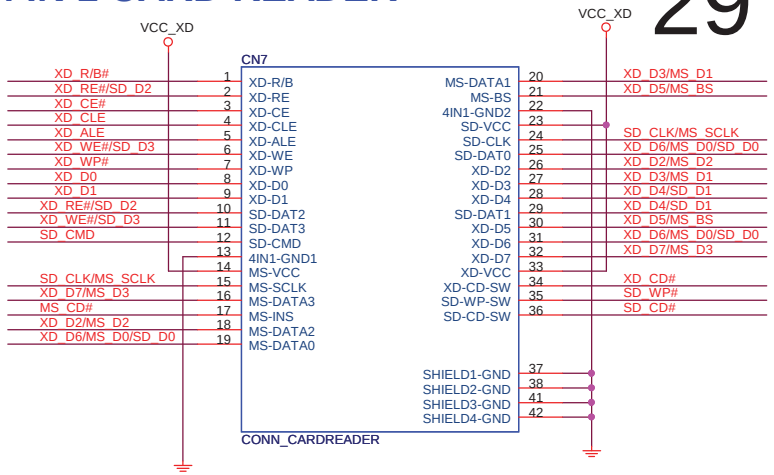
(MMC)

4 IN 1 CARD READER

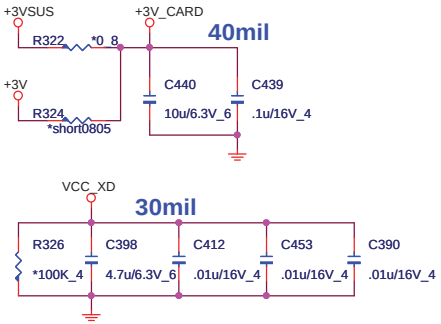
29



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal



CARDREADER POWER



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	CARD READER RTS5159	1A

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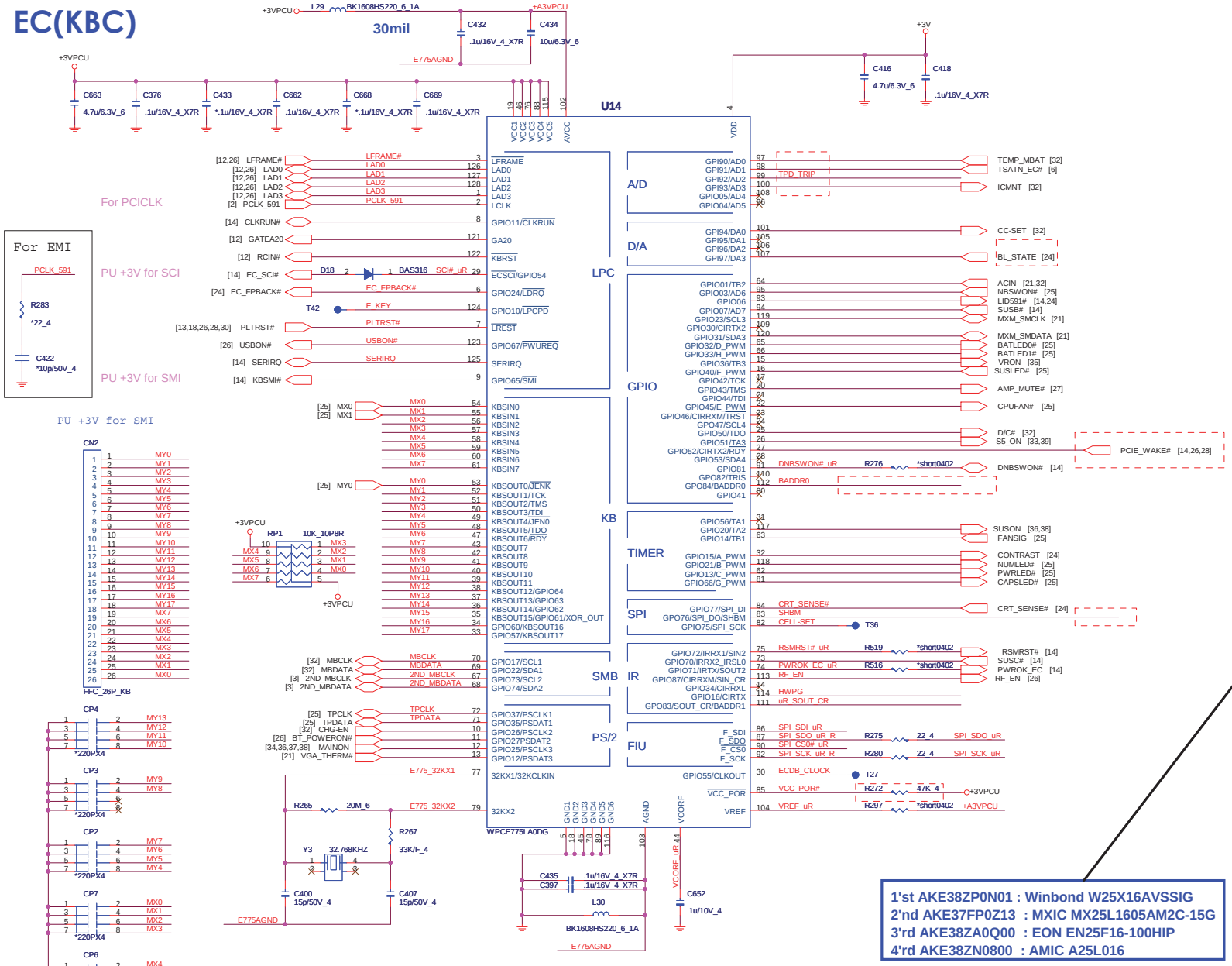
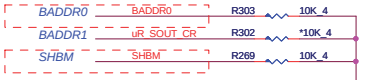
EC(KBC)



I/O ADDRESS SETTING

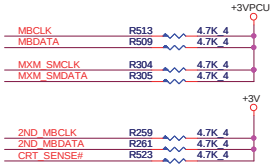
	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

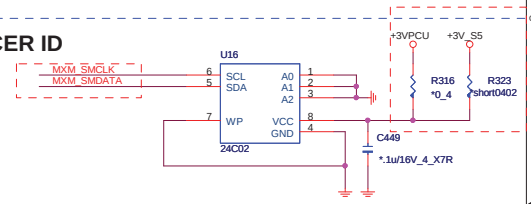


1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

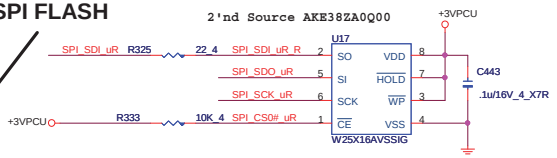


ACER ID



SPI FLASH

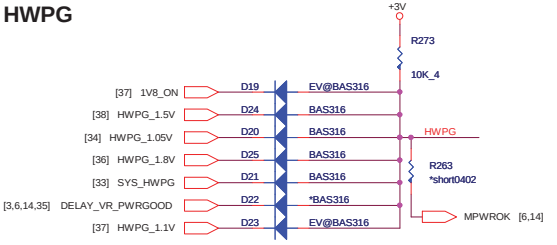
2'nd Source AKE38ZA0Q00



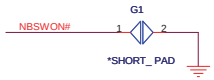
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

1'st AKE38ZP0N01 : Winbond W25X16AVSSIG
2'nd AKE37FP0Z13 : MXIC MX25L1605AM2C-15G
3'rd AKE38ZA0Q00 : EON EN25F16-100HIP
4'rd AKE38ZN0800 : AMIC A25L016

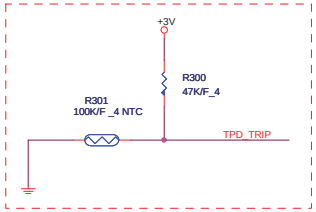
HWPG



POWER-ON PAD(UIF)



Thermal Sensor(THM)



INTERNAL KEYBOARD STRIP SET

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

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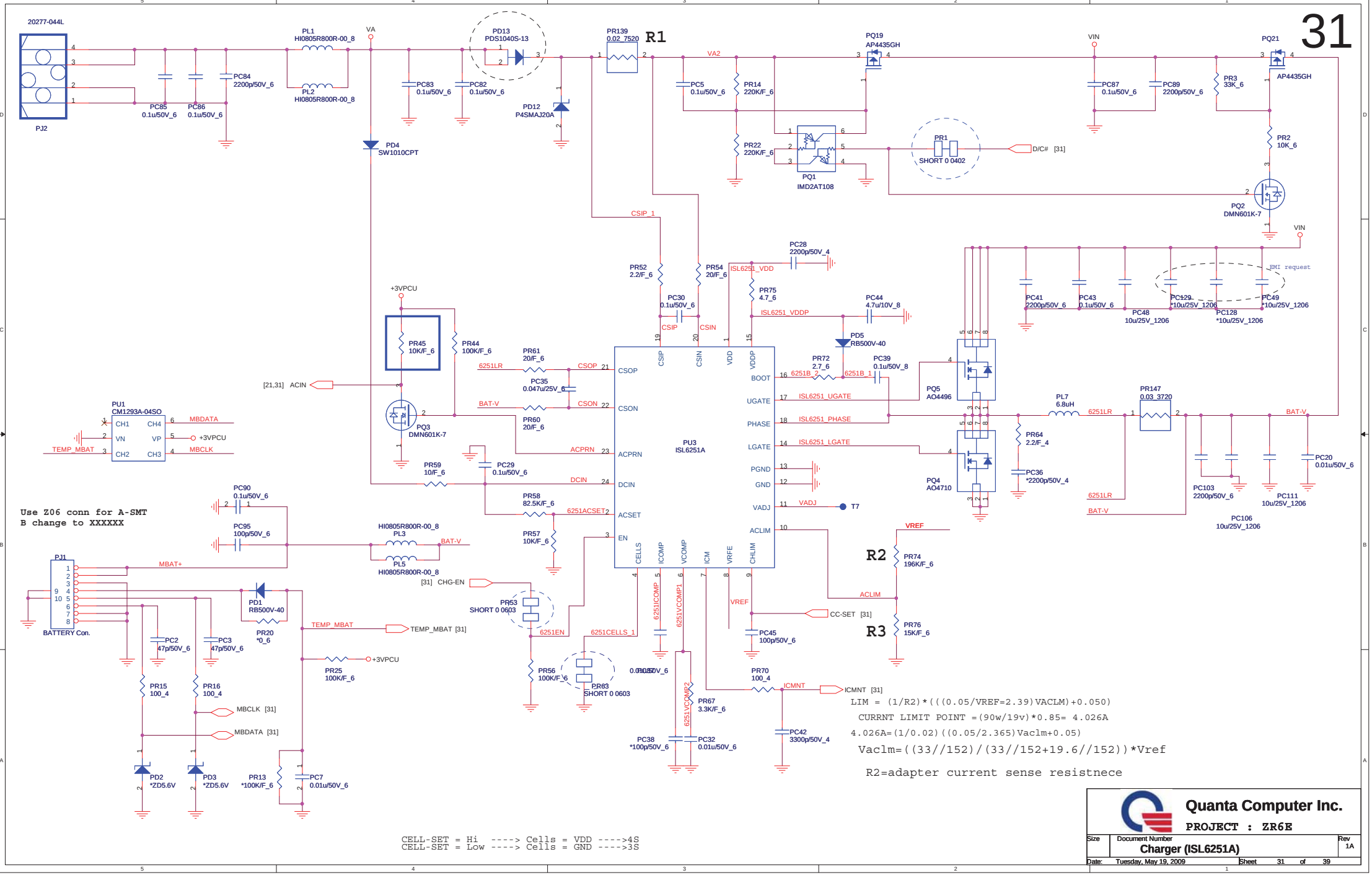
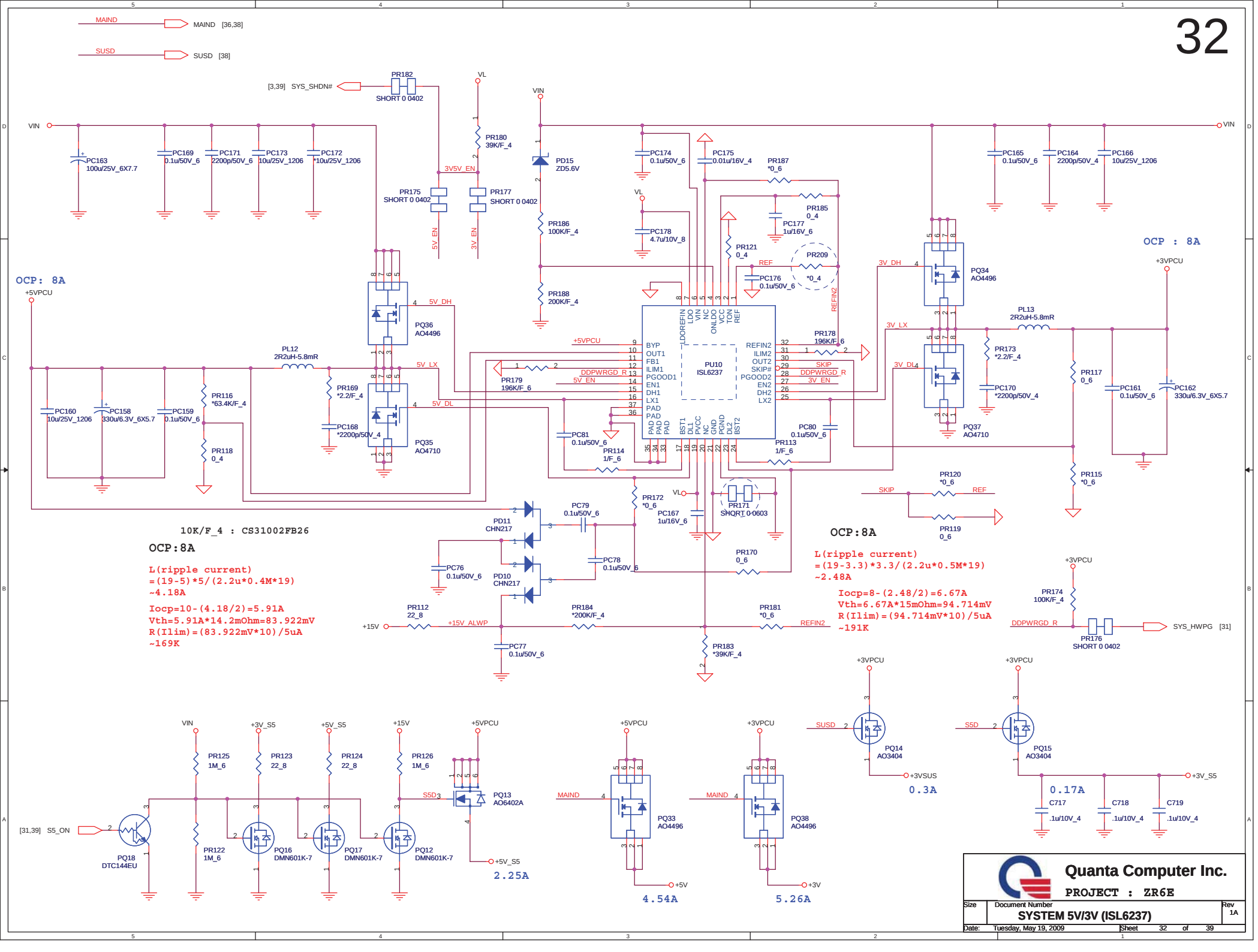


Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	Charger (ISL6251A)	1A

Date: Tuesday, May 19, 2009 Sheet 31 of 39



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	SYSTEM 5V/3V (ISL6237)	1A

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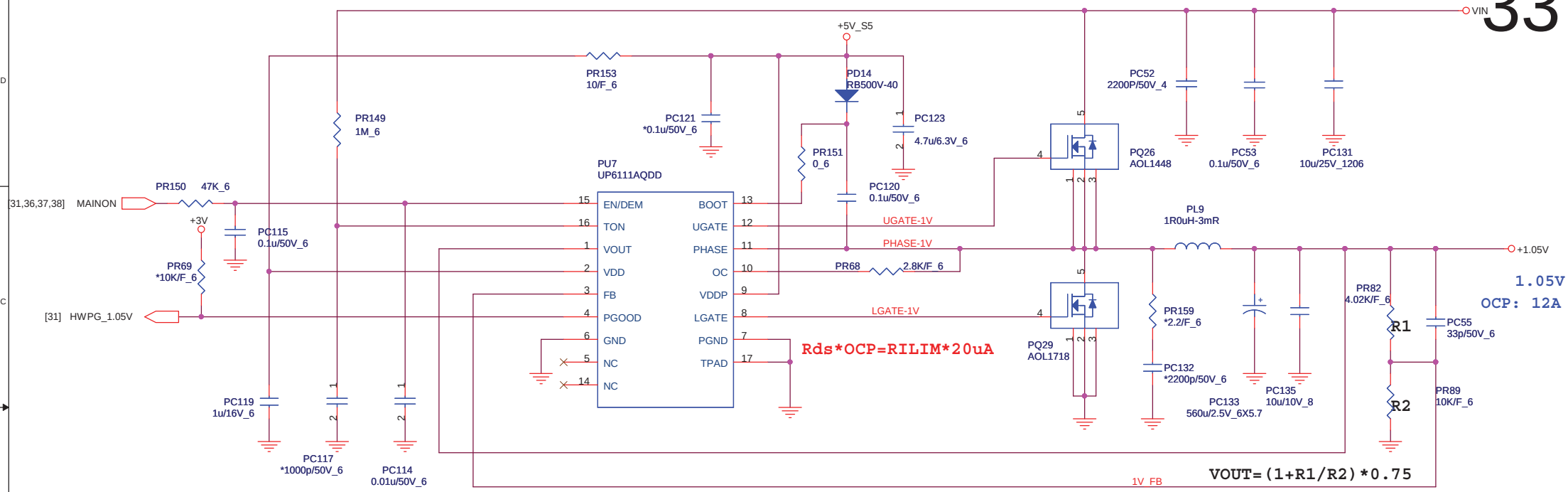


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AOL1412 Rdson=4.6mOhm

OCP=16-0.8A

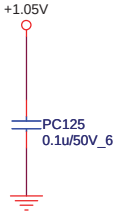
L(ripple current)

=(19-1.05)*1.05/(1u*272k*19)

~3.646A

4.6m*12=RILIM*20uA

RILIM=2.76K--- 2.8K



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	1A

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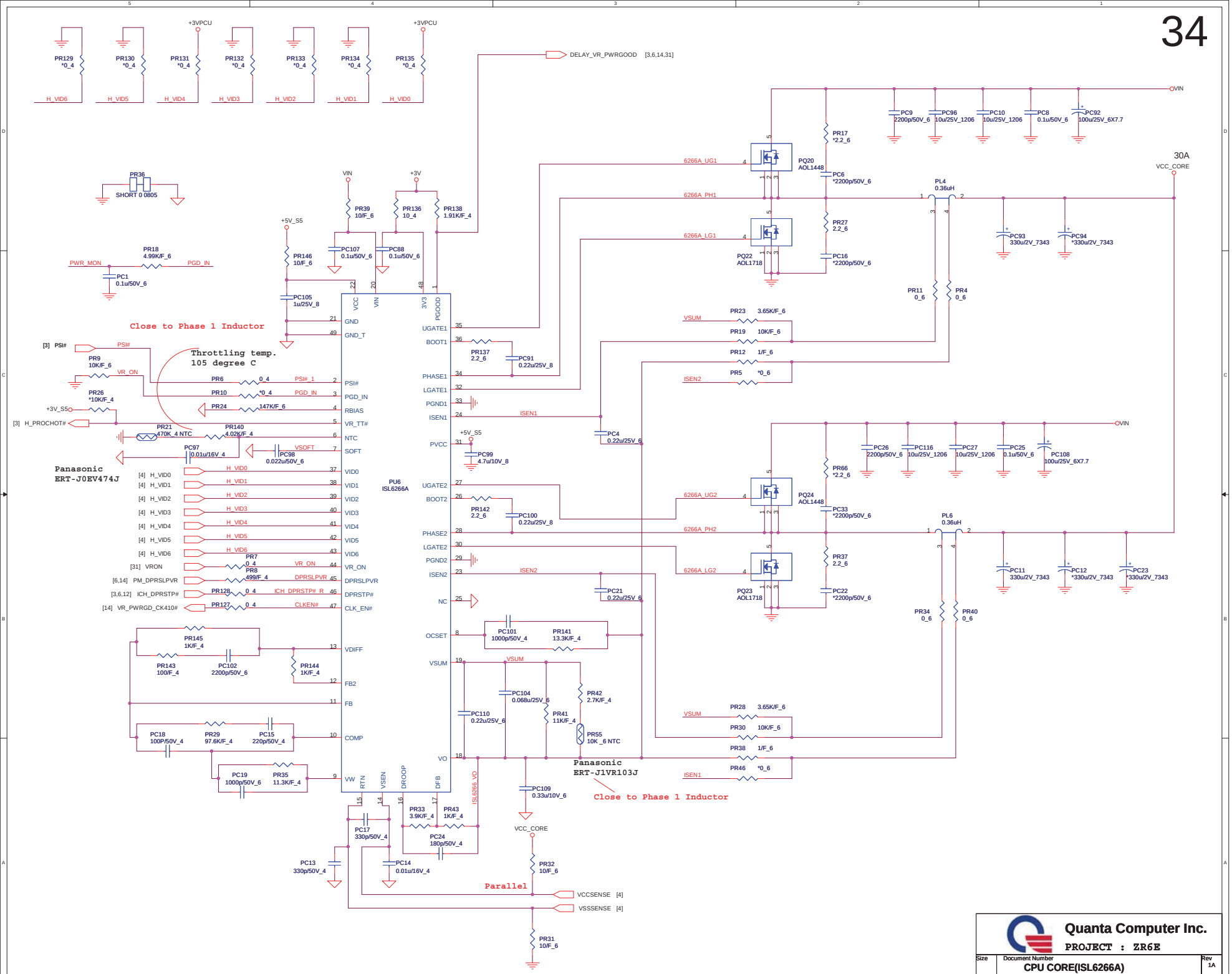

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	CPU CORE(ISL6266A)	1A

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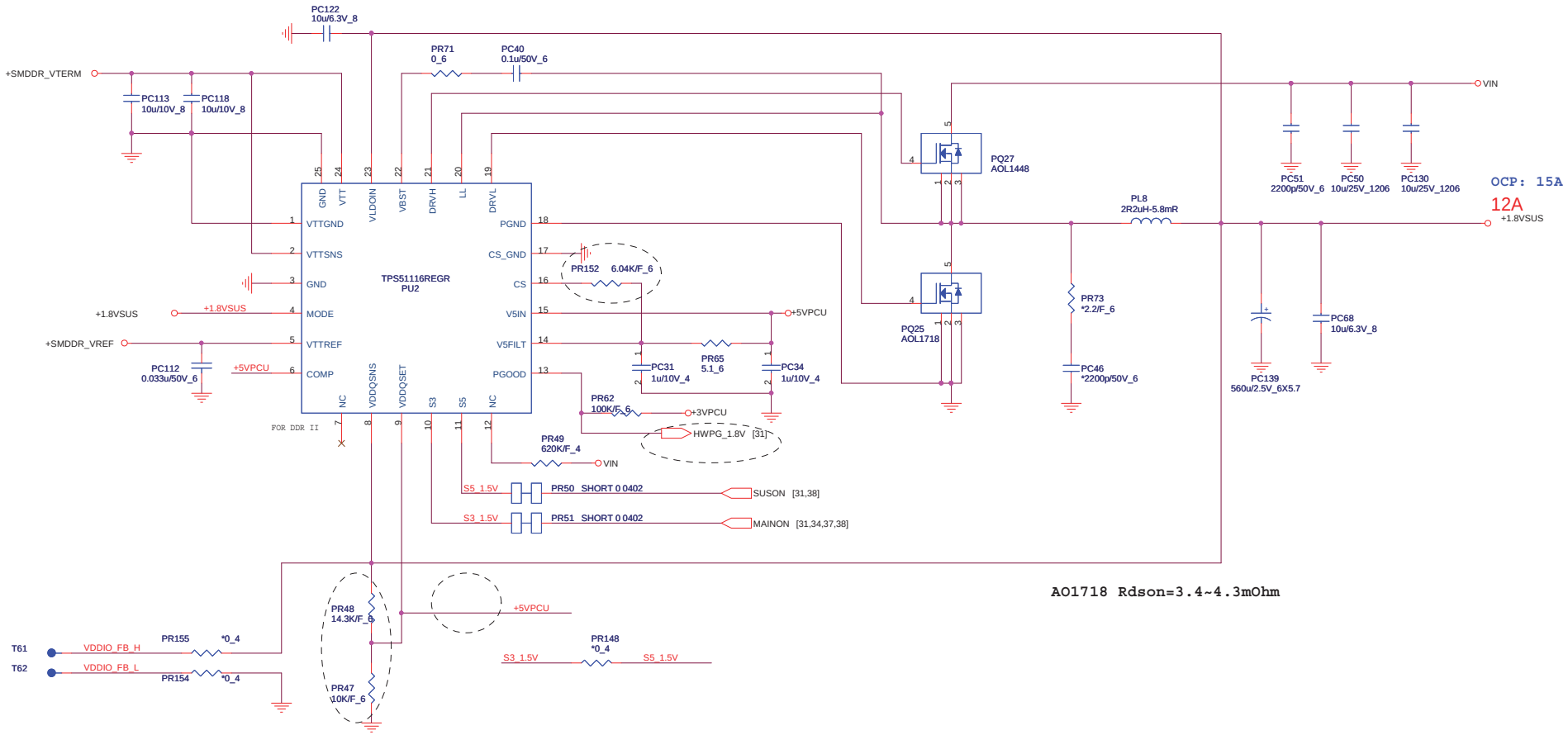
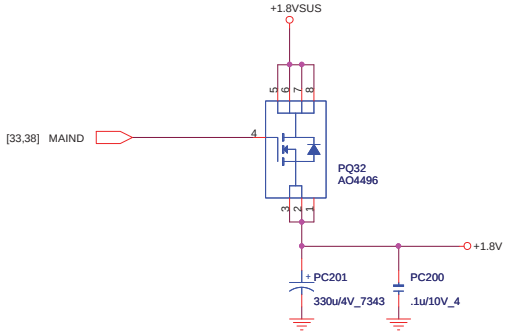


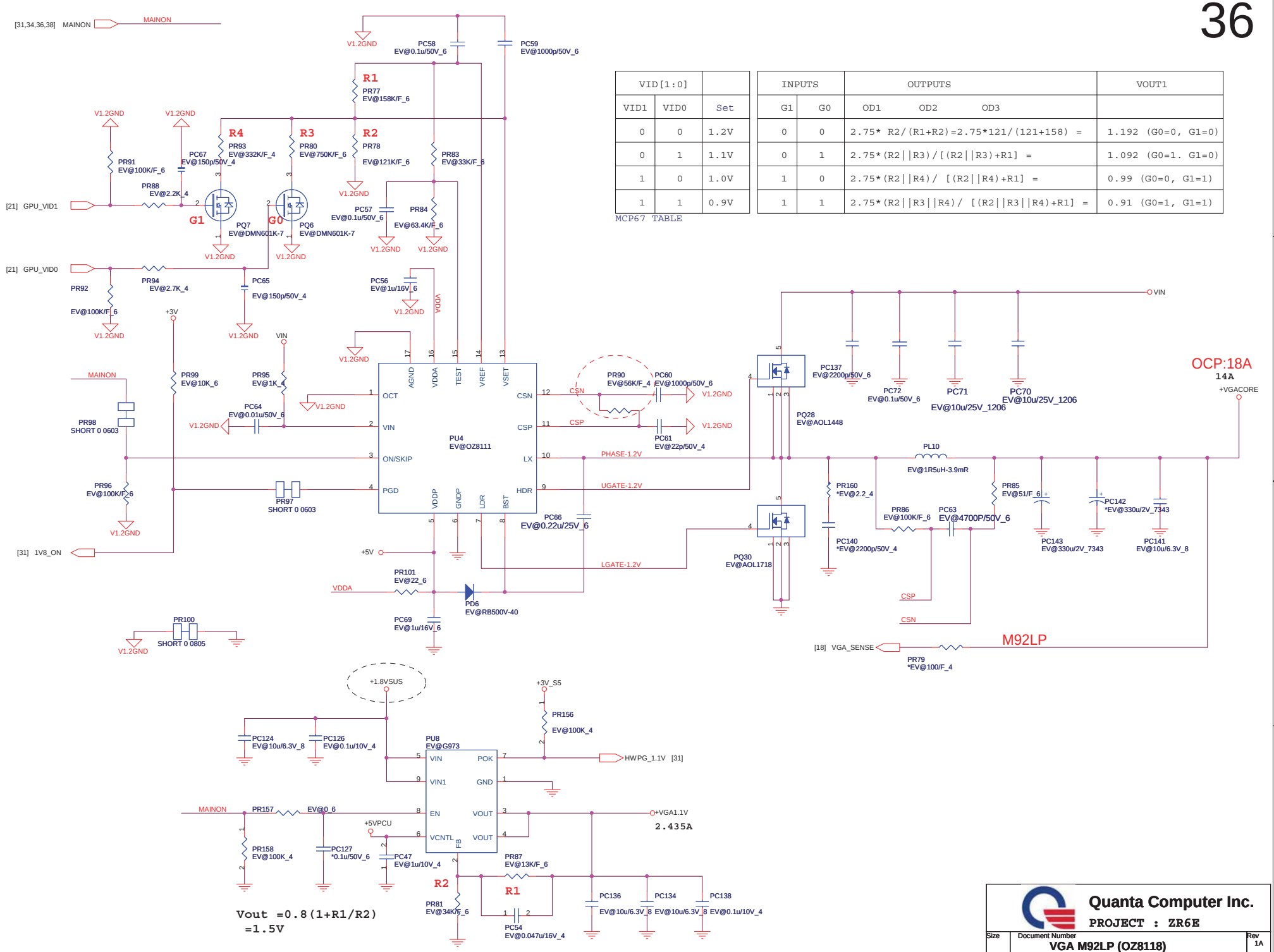


Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

Date: Wednesday, May 20, 2009 Sheet 35 of 39



VID[1:0]		
VID1	VID0	Set
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

MCP67 TABLE

INPUTS		OUTPUTS			VOUT1
G1	G0	OD1	OD2	OD3	
0	0	2.75* R2/(R1+R2)=2.75*121/(121+158) =			1.192 (G0=0, G1=0)
0	1	2.75*(R2||R3)/[(R2||R3)+R1] =			1.092 (G0=1. G1=0)
1	0	2.75*(R2||R4)/ [(R2||R4)+R1] =			0.99 (G0=0, G1=1)
1	1	2.75*(R2||R3||R4)/ [(R2||R3||R4)+R1] =			0.91 (G0=1, G1=1)

Quanta Computer Inc.

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Size	Document Number	Rev
	VGA M92LP (OZ8118)	1A

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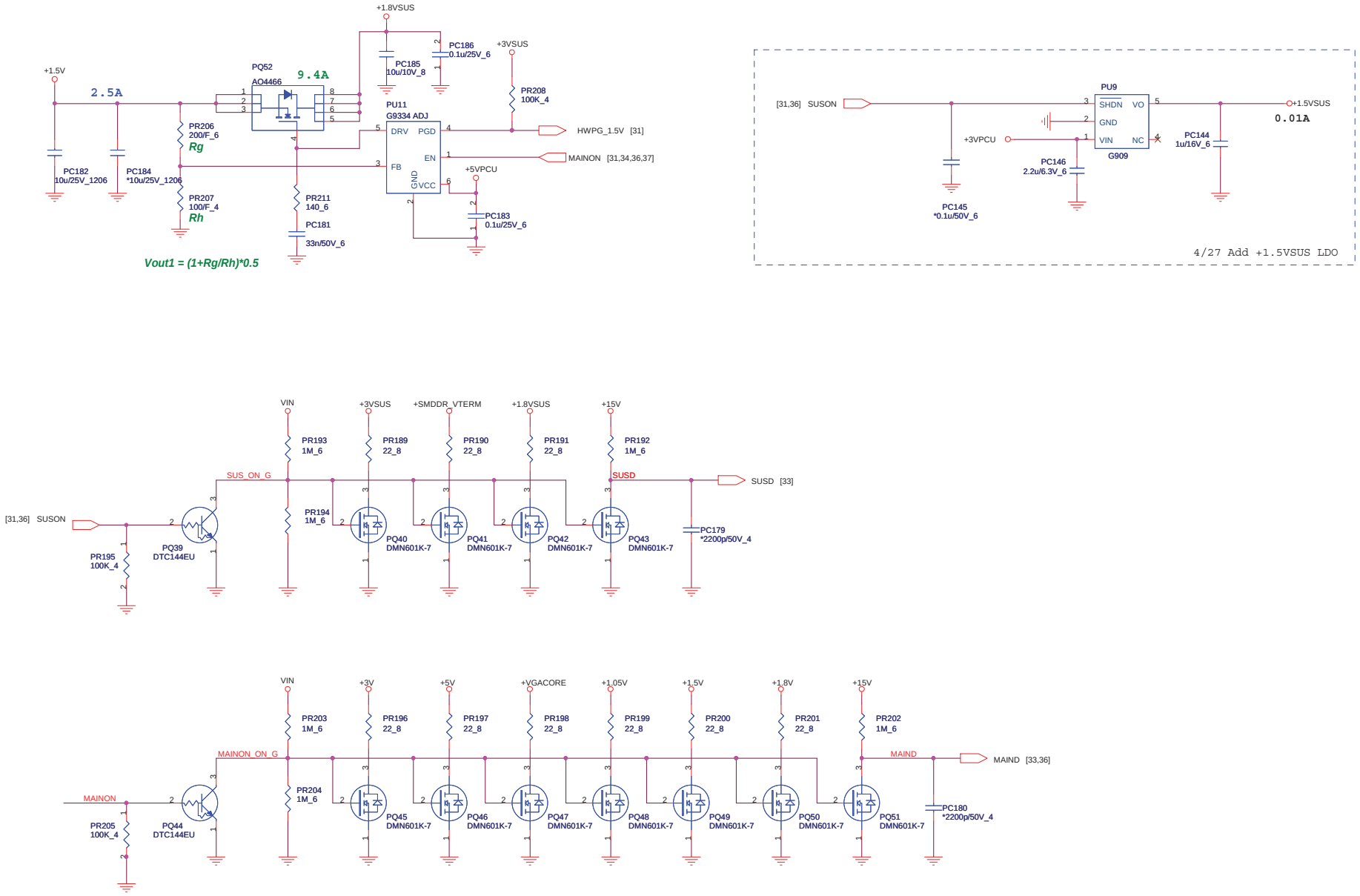

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	Discharge	1A

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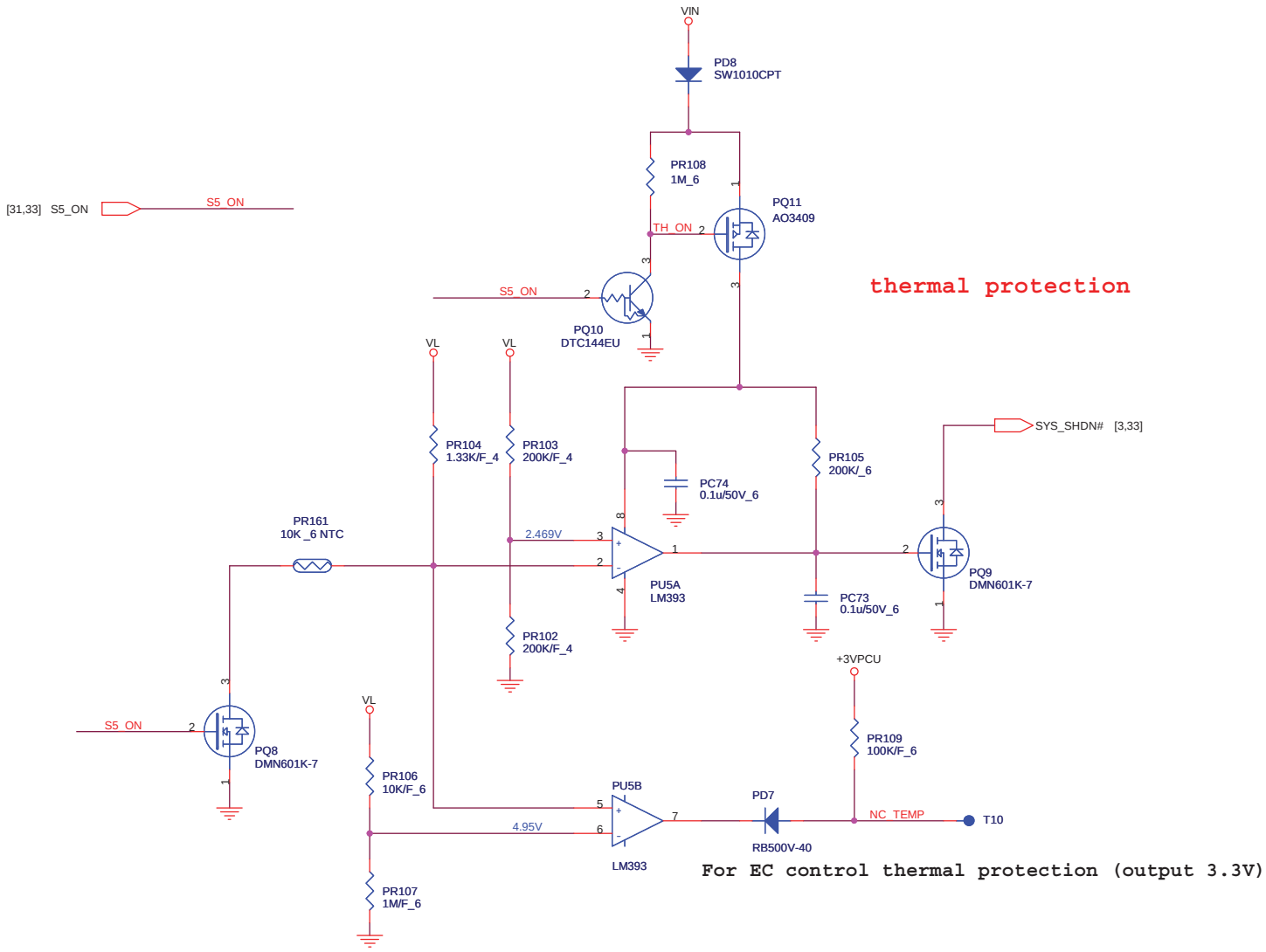

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.

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Size	Document Number	Rev
	Thermal Protection	1A

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MODEL:	REV
ZR6 MB	

CHANGE LIST

PAGE \ MODEL	ZR6 MB FROM	ZR6 MB TO
1	1A	
2	1A	3B
3	1A	
4	1A	
5	2A	
6	1A	
7	1A	
8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B
40		

MB Assy' P/N: 31ZR6MB00B0,C0,D0,E0,F0,G0	Project :ZR6E MB	Document No.:
Approved by :	Drawing by : James Chen	DATE:

Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	Thermal Protection	1A

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